

Multiprocessor Hardware A computer system in which two or more CPUs share full access to the main memory Each CPU might have its own cache and the coherence among multiple cache is maintained • write operation by a CPU is visible to all other CPUs writes to the same location is seen in the same order by all CPUs (also called write serialization) CPU CPU CPU Cache Cache Cache Memory bus Memory bus snooping and cache invalidation

CSC 256/456 - Spring 2006

2

4/4/2007













Protecting short cr Disabling interru Software spin loc Hardware spin lo using TSL	itical region – busy waiting is OK pts does not work cks cks
entry section:	
TSL R1, LOCK	copy lock to R1 and set lock to 1
CMP R1, #0	was lock zero?
JNE entry_section	if it wasn't zero, lock was set, so loop
RET	return; critical section entered
exit_section:	
MOV LOCK, #0	store 0 into lock
RET	return; out of critical section
4/4/2007	CSC 256/456 - Spring 2006 9

TSL on Multiprocessor

- TSL involves two actions (reading the value and writing 1) and it needs to be atomic
- On uniprocessor, we simply need to make the two actions unbreakable
- On multiprocessor, the TSL implementation is more complex, usually it has to monopolize the memory bus













Disclaimer Parts of the lecture slides contain original work by Andrew S. Tanenbaum. The slides are intended for the sole purpose of instruction of operating systems at the University of Rochester. All copyrighted materials belong to their original owner(s).