SPARC V7.0

Instruction Set

for Embedded Real time 32–bit Computer
(ERC32)
for SPACE Applications
1. Assembly Language Syntax

The notations given in this section are taken from Sun’s SPARC Assembler and are used to describe the suggested assembly language syntax for the instruction definitions given in Section 6.2.

Understanding the use of type fonts is crucial to understanding the assembly language syntax in the instruction definitions. Items in typewriter font are literals, to be entered exactly as they appear. Items in italic font are metasymbols that are to be replaced by numeric or symbolic values when actual assembly language code is written. For example, asi would be replaced by a number in the range of 0 to 255 (the value of the bits in the binary instruction), or by a symbol that has been bound to such a number.

Subscripts on metasymbols further identify the placement of the operand in the generated binary instruction. For example, regs2 is a reg (i.e., register name) whose binary value will end up in the rs2 field of the resulting instruction.

1.1. Register Names

reg

A reg is an integer unit register. It can have a value of:

<table>
<thead>
<tr>
<th>%0 through %31</th>
<th>all integer registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>%g0 through %g7</td>
<td>global registers—same as %0 through %7</td>
</tr>
<tr>
<td>%o0 through %o7</td>
<td>out registers—same as %8 through %15</td>
</tr>
<tr>
<td>%l0 through %l7</td>
<td>local registers—same as %16 through %23</td>
</tr>
<tr>
<td>%i0 through %i7</td>
<td>in registers—same as %24 through %31</td>
</tr>
</tbody>
</table>

Subscripts further identify the placement of the operand in the binary instruction as one of the following:

- reg—rs1 field
- reg—rs2 field
- reg—rd field

freg

A freg is a floating-point register. It can have a value from %f0 through %f31. Subscripts further identify the placement of the operand in the binary instruction as one of the following:

- fre—rs1 field
- fre—rs2 field
- fre—rd field

creg

A creg is a coprocessor register. It can have a value from %c0 through %c31. Subscripts further identify the placement of the operand in the binary instruction as one of the following:

- creg—rs1 field
- creg—rs2 field
- creg—rd field

1.2. Special Symbol Names

Certain special symbols need to be written exactly as they appear in the syntax table. These appear in typewriter font, and are preceded by a percent sign (%). The percent sign is part of the symbol name; it must appear as part of the literal value.
The symbol names are:

- %psr: Processor State Register
- %wim: Window Invalid Mask register
- %tbr: Trap Base Register
- %y: Y register
- %fpr: Floating-point State Register
- %cpr: Coprocessor State Register
- %fpq: Floating-point Queue
- %cpq: Coprocessor Queue
- %hi: Unary operator that extracts high 22 bits of its operand
- %lo: Unary operator that extracts low 10 bits of its operand

1.3. Values

Some instructions use operands comprising values as follows:

- simm13: A signed immediate constant that fits in 13 bits
- const22: A constant that fits in 22 bits
- asi: An alternate address space identifier (0 to 255)

1.4. Label

A label is a sequence of characters comprised of alphabetic letters (a–z, A–Z (upper and lower case distinct)), underscore (_), dollar sign ($), period (.), and decimal digits (0–9), but which does not begin with a decimal digit.

Some instructions offer a choice of operands. These are grouped as follows:

- regaddr:
  - reg
  - reg + reg

- address:
  - reg
  - reg + reg
  - reg + simm13
  - reg - simm13
  - simm13
  - simm13 + reg

- reg_or_imm:
  - reg
  - simm13

1.5. Instruction Mnemonics

Figure 1.1 illustrates the mnemonics used to describe the SPARC instruction set. Note that some combinations possible in Figure 1.1 do not correspond to valid instructions (such as store signed or floating-point convert extended to extended). Refer to the instruction summary on page 6–6 for a list of valid SPARC instructions.
Data Transfer

Integer Operations

Floating-Point Operations

Control Transfer

Figure 1.1. SPARC Instruction Mnemonic Summary
2. Definitions

This section provides a detailed definition for each CY7C601 instruction. Each definition includes: the instruction operation; suggested assembly language syntax; a description of the salient features, restrictions and trap conditions; a list of synchronous or floating-point/coprocessor traps which can occur as a consequence of executing the instruction; and the instruction format and op codes. Instructions are defined in alphabetical order with the instruction mnemonic shown in large bold type at the top of the page for easy reference. The instruction set summary that precedes the definitions, (Table 1.2), groups the instructions by type.

Table 1.1 identifies the abbreviations and symbols used in the instruction definitions. An example of how some of the description notations are used is given below in Figure 1.2. Register names, labels and other aspects of the syntax used in these instructions are described in the previous section.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Instruction field that controls instruction annulling during control transfers</td>
</tr>
<tr>
<td>AND, OR, XOR, etc.</td>
<td>AND, OR, XOR, etc operators</td>
</tr>
<tr>
<td>asr_reg</td>
<td>Any implemented ASR (Ancillary State)</td>
</tr>
<tr>
<td>c</td>
<td>The icc carry bit</td>
</tr>
<tr>
<td>ccc</td>
<td>The coprocessor condition code field of the CCSR</td>
</tr>
<tr>
<td>CONCAT</td>
<td>Concatenate</td>
</tr>
<tr>
<td>cond</td>
<td>Instruction field that selects the condition code test for branches</td>
</tr>
</tbody>
</table>

![Figure 1.2. Instruction Description](image-url)
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>creg</td>
<td>Communication Coprocessor Register: can be %ccsr, %ccfr, %ccpr, %ccccr</td>
</tr>
<tr>
<td>CWP</td>
<td>PSR's Current Window Pointer field</td>
</tr>
<tr>
<td>disp22</td>
<td>Instruction field that contains the 22-bit sign-extended displacement for branches</td>
</tr>
<tr>
<td>disp30</td>
<td>Instruction field that contains the 30-bit word displacement for calls</td>
</tr>
<tr>
<td>EC</td>
<td>PSR's Enable Coprocessor bit</td>
</tr>
<tr>
<td>EF</td>
<td>PSR's Enable FPU bit</td>
</tr>
<tr>
<td>ET</td>
<td>PSR's Enable Traps bit</td>
</tr>
<tr>
<td>i</td>
<td>Instruction field that selects rs2 or signExtend(simm13) as the second operand</td>
</tr>
<tr>
<td>icc</td>
<td>The integer condition code field of the PSR</td>
</tr>
<tr>
<td>imm22</td>
<td>Instruction field that contains the 22-bit constant used by SETHI</td>
</tr>
<tr>
<td>n</td>
<td>The icc negative bit</td>
</tr>
<tr>
<td>not</td>
<td>Logical complement operator</td>
</tr>
<tr>
<td>nPC</td>
<td>Next Program Counter</td>
</tr>
<tr>
<td>opc</td>
<td>Instruction field that specifies the count for Coprocessor-operate instructions</td>
</tr>
<tr>
<td>operand2</td>
<td>Either r[rs2] or signExtend(simm13)</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>pS</td>
<td>PSR's previous Supervisor bit</td>
</tr>
<tr>
<td>PSR</td>
<td>Processor State Register</td>
</tr>
<tr>
<td>r[15]</td>
<td>A directly addressed register (could be floating-point or coprocessor)</td>
</tr>
<tr>
<td>rd</td>
<td>Instruction field that specifies the destination register (except for store)</td>
</tr>
<tr>
<td>r[rd]</td>
<td>Depending on context, the integer register (or its contents) specified by the instruction field, e.g., rd, rs1, rs2</td>
</tr>
<tr>
<td>r[rd]&lt;31&gt;</td>
<td>&lt;&gt; are used to specify bit fields of a particular register or I/O signal</td>
</tr>
<tr>
<td>[r[rs1] + r[rs2]]</td>
<td>The contents of the address specified by r[rs1] + r[rs2]</td>
</tr>
<tr>
<td>rs1</td>
<td>Instruction field that specifies the source 1 register</td>
</tr>
<tr>
<td>rs2</td>
<td>Instruction field that specifies the source 2 register</td>
</tr>
<tr>
<td>S</td>
<td>PSR's Supervisor bit</td>
</tr>
<tr>
<td>shcnt</td>
<td>Instruction field that specifies the count for shift instructions</td>
</tr>
<tr>
<td>signExtend(simm13)</td>
<td>Instruction field that contains the 13-bit, sign-extended immediate value</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBR</td>
<td>Trap Base Register</td>
</tr>
<tr>
<td>tt</td>
<td>TBR's trap type field</td>
</tr>
<tr>
<td>uf</td>
<td>Floating-point exception: underflow</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------------------------------------</td>
</tr>
<tr>
<td>v</td>
<td>The icc overflow bit</td>
</tr>
<tr>
<td>WIM</td>
<td>Window Invalid Mask register</td>
</tr>
<tr>
<td>Y</td>
<td>Y Register</td>
</tr>
<tr>
<td>z</td>
<td>The icc zero bit</td>
</tr>
<tr>
<td>-</td>
<td>Subtract</td>
</tr>
<tr>
<td>x</td>
<td>Multiply</td>
</tr>
<tr>
<td>/</td>
<td>Divide</td>
</tr>
<tr>
<td>&lt;--</td>
<td>Replaced by</td>
</tr>
<tr>
<td>7FFFFFF H</td>
<td>Hexadecimal number representation</td>
</tr>
<tr>
<td>+</td>
<td>Add</td>
</tr>
<tr>
<td>Name</td>
<td>Operation</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>------------------------------------------------</td>
</tr>
<tr>
<td>LDBH(LDDBA)</td>
<td>Load Signed Byte</td>
</tr>
<tr>
<td>LDBH(LDDBA)</td>
<td>Load Signed Halfword</td>
</tr>
<tr>
<td>LDUB(LDUBA)</td>
<td>Load Unsigned Byte</td>
</tr>
<tr>
<td>LDUB(LDUBA)</td>
<td>Load Unsigned Halfword</td>
</tr>
<tr>
<td>LDLD(LDLD)</td>
<td>Load Word</td>
</tr>
<tr>
<td>LDLD(LDLD)</td>
<td>Load Doubleword</td>
</tr>
<tr>
<td>LDF</td>
<td>Load Floating Point</td>
</tr>
<tr>
<td>LDF</td>
<td>Load Double Floating Point</td>
</tr>
<tr>
<td>LDFSR</td>
<td>Load Floating Point State Register</td>
</tr>
<tr>
<td>STB(STBA)</td>
<td>Store Byte</td>
</tr>
<tr>
<td>STB(STBA)</td>
<td>Store Halfword</td>
</tr>
<tr>
<td>ST(WSTA)</td>
<td>Store Word</td>
</tr>
<tr>
<td>ST(WSTA)</td>
<td>Store Doubleword</td>
</tr>
<tr>
<td>LDSTU(LDSTUBA)</td>
<td>Load Signed/Store Signed Byte</td>
</tr>
<tr>
<td>LDSTU(LDSTUBA)</td>
<td>Load Signed/Store Signed Halfword</td>
</tr>
<tr>
<td>LDSTU(LDSTUBA)</td>
<td>Load Unsigned/Store Unsigned Byte</td>
</tr>
<tr>
<td>LDSTU(LDSTUBA)</td>
<td>Load Unsigned/Store Unsigned Halfword</td>
</tr>
<tr>
<td>LDSTU(LDSTUBA)</td>
<td>Load Doubleword</td>
</tr>
<tr>
<td>ADD(ADDXc)</td>
<td>Add</td>
</tr>
<tr>
<td>ADD(ADDXc)</td>
<td>Add with Carry</td>
</tr>
<tr>
<td>ADDX(ADDXc)</td>
<td>Add</td>
</tr>
<tr>
<td>ADDX(ADDXc)</td>
<td>Add with Carry</td>
</tr>
<tr>
<td>ADDX(ADDXc)</td>
<td>Add</td>
</tr>
<tr>
<td>ADDX(ADDXc)</td>
<td>Add with Carry</td>
</tr>
<tr>
<td>TADDx(TADDxTv)</td>
<td>Tagged Add and modify icc</td>
</tr>
<tr>
<td>SUB(SUBcc)</td>
<td>Subtract</td>
</tr>
<tr>
<td>SUB(SUBcc)</td>
<td>Subtract with Carry</td>
</tr>
<tr>
<td>MULTx</td>
<td>Multiply Step and modify icc</td>
</tr>
<tr>
<td>AND(ANDXc)</td>
<td>And</td>
</tr>
<tr>
<td>AND(ANDXc)</td>
<td>And Not</td>
</tr>
<tr>
<td>AND(ANDXc)</td>
<td>And Not</td>
</tr>
<tr>
<td>OR(ORGcc)</td>
<td>OR(ORGcc)</td>
</tr>
<tr>
<td>OR(ORGcc)</td>
<td>OR(ORGcc)</td>
</tr>
<tr>
<td>XOR(XORRcc)</td>
<td>XOR(XORRcc)</td>
</tr>
<tr>
<td>XOR(XORRcc)</td>
<td>XOR(XORRcc)</td>
</tr>
<tr>
<td>XOR(XORRcc)</td>
<td>XOR(XORRcc)</td>
</tr>
<tr>
<td>SLG</td>
<td>Shift Logical</td>
</tr>
<tr>
<td>SRL</td>
<td>Shift Right Logical</td>
</tr>
<tr>
<td>SRA</td>
<td>Shift Right Arithmetic</td>
</tr>
<tr>
<td>SETH</td>
<td>Set High 32 Bits of r Register</td>
</tr>
<tr>
<td>SAVE</td>
<td>Save caller’s window</td>
</tr>
<tr>
<td>RESTORE</td>
<td>Restore caller’s window</td>
</tr>
<tr>
<td>Bicc</td>
<td>Branch on Integer Condition Codes</td>
</tr>
<tr>
<td>Fbicc</td>
<td>Branch on Floating Point Condition Codes</td>
</tr>
<tr>
<td>Cbicc</td>
<td>Branch on Coprocessor Condition Codes</td>
</tr>
<tr>
<td>CALL</td>
<td>Call</td>
</tr>
<tr>
<td>JMP</td>
<td>Jump and Link</td>
</tr>
<tr>
<td>RTH</td>
<td>Return from trap</td>
</tr>
<tr>
<td>TRAP</td>
<td>Trap on Integer Condition Codes</td>
</tr>
<tr>
<td>RDY</td>
<td>Read Y Register</td>
</tr>
<tr>
<td>RDPsR*</td>
<td>Read Processor State Register</td>
</tr>
<tr>
<td>RDIWM*</td>
<td>Read Window Invalid Mask</td>
</tr>
<tr>
<td>RDTBR*</td>
<td>Read Trap Base Register</td>
</tr>
<tr>
<td>WRY</td>
<td>Write Y Register</td>
</tr>
<tr>
<td>WRPSR*</td>
<td>Write Processor State Register</td>
</tr>
<tr>
<td>WRIWM*</td>
<td>Write Window Invalid Mask</td>
</tr>
<tr>
<td>WRTRBR*</td>
<td>Write Trap Base Register</td>
</tr>
<tr>
<td>UNIMF</td>
<td>Unimplemented Instruction</td>
</tr>
<tr>
<td>IFUSH</td>
<td>Instruction Cache Flush</td>
</tr>
<tr>
<td>FPU</td>
<td>Floating Point Unit Operations</td>
</tr>
<tr>
<td>CPOp*</td>
<td>Coprocessor Operations</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FP Op Type</th>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPU</td>
<td>Floating Point Unit Operations</td>
<td>1 to Launch</td>
</tr>
<tr>
<td>CPOp*</td>
<td>Coprocessor Operations</td>
<td>1 to Launch</td>
</tr>
</tbody>
</table>

* privileged instruction
** assuming delay slots are filled with useful instructions
ADD

Operation: \( r[rd] \leftarrow r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) \)

Assembler Syntax: `add reg(rs1), reg_or_imm, reg(rd)`

Description: The ADD instruction adds the contents of the register named in the `rs1` field, \( r[rs1] \), to either the contents of \( r[rs2] \) if the instruction’s `i` bit equals zero, or to the 13-bit, sign-extended immediate operand contained in the instruction if `i` equals one. The result is placed in the register specified in the `rd` field.

Traps: none

Format:

\[
\begin{array}{cccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
& & & & & & & & & & & & & & & \\
1 & 0 & rd & 0 & 0 & 0 & 0 & 0 & rs1 & i=0 & ignored & & & & rs2 \\
\end{array}
\]

\[
\begin{array}{cccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
& & & & & & & & & & & & & & & \\
1 & 0 & rd & 0 & 0 & 0 & 0 & 0 & rs1 & i=1 & & & & simm13 \\
\end{array}
\]
ADDcc  

Add and modify icc

**Operation:**  
\[ r[rd] \leftarrow r[rs1] + \text{operand2}, \text{where operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]

- **n**: \( r[rd]<31> \)
- **z**: if \( r[rd] = 0 \) then 1, else 0
- **v**: \((r[rs1]<31> \text{ AND operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND not } \text{operand2}<31> \text{ AND } r[rd]<31>)\)
- **c**: \((r[rs1]<31> \text{ AND operand2}<31>) \text{ OR (not } r[rd]<31> \text{ AND (} r[rs1]<31> \text{ OR operand2}<31>)\)

**Assembler Syntax:**  
ADDcc \( reg_{rs1}, reg_{or_imm}, reg_{rd} \)

**Description:** ADDcc adds the contents of \( r[rs1] \) to either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or to a 13-bit, sign-extended immediate operand if \( i \) equals one. The result is placed in the register specified in the \( rd \) field. In addition, ADDcc modifies all the integer condition codes in the manner described above.

**Traps:** none

**Format:**

```
<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>i=0</td>
<td>ignored</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
ADDX

Add with Carry

Operation:  
\[ r[rd] \leftarrow r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) + c \]

Assembler Syntax:  
`addx reg_rs1, reg_or_imm, reg_rd`

Description:  
ADDX adds the contents of \( r[rs1] \) to either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or to a 13-bit, sign-extended immediate operand if \( i \) equals one. It then adds the PSR’s carry bit (c) to that result. The final result is placed in the register specified in the \( rd \) field.

Traps:  
none

Format:

\[
\begin{array}{c|cccc|cc|ccc|c}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 0 & rd & 0 & 0 & 1 & 0 & 0 & 0 & rs1 & i=0 & ignored & rs2 \\
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
\hline
1 & 0 & rd & 0 & 0 & 1 & 0 & 0 & 0 & rs1 & i=1 & simm13 \\
\end{array}
\]
**ADDXcc**

**Operation:**

\[ r[rd] \leftarrow r[rs1] + \text{operand2} + c, \text{ where } \text{operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]

\[ n \leftarrow r[rd]<31> \]

\[ z \leftarrow \text{if } r[rd] = 0 \text{ then } 1, \text{ else } 0 \]

\[ v \leftarrow (r[rs1]<31> \text{ AND operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND not operand2}<31> \text{ AND } r[rd]<31>) \]

\[ c \leftarrow (r[rs1]<31> \text{ AND operand2}<31>) \text{ OR (not } r[rd]<31> \text{ AND (r[rs1]<31> OR operand2}<31>)) \]

**Assembler Syntax:**

```
addxcc reg, reg_or_imm, reg
```

**Description:**

ADDXcc adds the contents of \( r[rs1] \) to either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or to a 13-bit, sign-extended immediate operand if \( i \) equals one. It then adds the PSR’s carry bit (c) to that result. The final result is placed in the register specified in the \( rd \) field. ADDXcc also modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

```
  31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
  01 01 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

```
  31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
  01 01 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

MATRA MHS
Rev. A (10/09/96)
### AND

**Operation:**
\[ r[rd] \leftarrow r[rs1] \ \text{AND} \ (r[rs2] \text{ or sign extnd(sim13)}) \]

**Assembler Syntax:**
```
and reg_rs1, reg_or_imm, reg_rd
```

**Description:**
This instruction does a bitwise logical AND of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

**Traps:**
none

**Format:**

```
<p>| | | | | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>19</td>
<td>18</td>
<td>14  \ 13  \ 12  \ 5  \ 4  \ 0</td>
</tr>
</tbody>
</table>
```

```
<p>| | | | | | | | | | | | | |</p>
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<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=1</td>
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<td></td>
</tr>
<tr>
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<td>29</td>
<td>28</td>
<td>27</td>
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<td>23</td>
<td>22</td>
<td>19</td>
<td>18</td>
<td>14  \ 13  \ 12  \ 5  \ 4  \ 0</td>
</tr>
</tbody>
</table>
```
ANDcc And and modify icc

Operation: \( r[rd] \leftarrow r[rs1] \ \text{AND} \ (r[rs2] \text{ or sign extnd(simm13)}) \)
\( n \leftarrow r[rd]<31> \)
\( z \leftarrow \) if \( r[rd] = 0 \) then 1, else 0
\( v \leftarrow 0 \)
\( c \leftarrow 0 \)

Assembler Syntax: `andcc reg_rs1, reg_or_imm, reg_rd`

Description: This instruction does a bitwise logical AND of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if if bit field \( i=1 \)). The result is stored in register \( r[rd] \). ANDcc also modifies all the integer condition codes in the manner described above.

Traps: none

Format:

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<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
</tr>
</tbody>
</table>

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<td>20</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
</tr>
</tbody>
</table>
**ANDN**  

**Operation:**  
\[ r[rd] \leftarrow r[rs1] \land (r[rs2] \lor \text{sign extnd(simm13)}) \]

**Assembler Syntax:**  
`andn rs1, reg_or_imm, rd`

**Description:**  
ANDN does a bitwise logical AND of the contents of register \(r[rs1]\) with the logical complement (not) of either \(r[rs2]\) (if if bit field \(i=0\)) or the 13-bit, sign-extended immediate value contained in the instruction (if if bit field \(i=1\)). The result is stored in register \(r[rd]\).

**Traps:**  
none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
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</thead>
<tbody>
<tr>
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<td>0</td>
<td>rd</td>
<td>000101</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
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<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ANDNcc

Operation:  
\[ r[rd] \leftarrow r[rs1] \text{ AND } (r[rs2] \text{ or sign extnd(simm13)}) \]
\[ n \leftarrow r[rd] < 31 > \]
\[ z \leftarrow \text{if } r[rd] = 0 \text{ then } 1, \text{ else } 0 \]
\[ v \leftarrow 0 \]
\[ c \leftarrow 0 \]

Assembler Syntax:  
`andncc reg(rd), reg_or_imm, reg rd`

Description:  
ANDNcc does a bitwise logical AND of the contents of register `r[rs1]` with the logical compliment (not) of either `r[rs2]` (if bit field `i=0`) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field `i=1`). The result is stored in register `r[rd]`. ANDNcc also modifies all the integer condition codes in the manner described above.

Traps:  
none

Format:  

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 0  | 1  | 0  | 1  | 0  | 1  | rs1 | i=0 | ignored | rs2 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1  | 0  | rd | 0  | 1  | 0  | 1  | 0  | 1  | rs1 | i=1 | simm13 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
**Bicc**

**Integer Conditional Branch**

**Operation:**

\[
\text{PC} \leftarrow \text{nPC}
\]

If condition true then
\[
\text{nPC} \leftarrow \text{PC} + (\text{sign extnd(disp22)} \times 4)
\]

else
\[
\text{nPC} \leftarrow \text{nPC} + 4
\]

**Assembler Syntax:**

- `ba{,a}`  
  - `label`
- `bn{,a}`  
  - `label`
- `bnc{,a}`  
  - `label`  
  - synonym: `bnz`
- `be{,a}`  
  - `label`  
  - synonym: `bz`
- `bg{,a}`  
  - `label`
- `ble{,a}`  
  - `label`
- `bge{,a}`  
  - `label`
- `bl{,a}`  
  - `label`
- `bgeu{,a}`  
  - `label`  
  - synonym: `bgeu`
- `bcs{,a}`  
  - `label`  
  - synonym: `bhu`
- `bpos{,a}`  
  - `label`
- `bneg{,a}`  
  - `label`
- `bvc{,a}`  
  - `label`
- `bvs{,a}`  
  - `label`

**Note:** The instruction’s annul bit field, \(a\), is set by appending “.a” after the branch name. If it is not appended, the \(a\) field is automatically reset. “.a” is shown in braces because it is optional.

**Description:**

The Bicc instructions (except for BA and BN) evaluate specific integer condition code combinations (from the PSR’s `icc` field) based on the branch type as specified by the value in the instruction’s `cond` field. If the specified combination of condition codes evaluates as true, the branch is taken, causing a delayed, PC-relative control transfer to the address \((\text{PC} + 4) + (\text{sign extnd(disp22)} \times 4)\). If the condition codes evaluate as false, the branch is not taken. Refer to Section NO TAG for additional information on control transfer instructions.

If the branch is not taken, the annul bit field (\(a\)) is checked. If \(a\) is set, the instruction immediately following the branch instruction (the delay instruction) is not executed (i.e., it is annulled). If the annul field is zero, the delay instruction is executed. If the branch is taken, the annul field is ignored, and the delay instruction is executed. See Section NO TAG regarding delay-branch instructions.

Branch Never (BN) executes like a NOP, except it obeys the annul field with respect to its delay instruction.

Branch Always (BA), because it always branches regardless of the condition codes, would normally ignore the annul field. Instead, it follows the same annul field rules: if \(a = 1\), the delay instruction is annulled; if \(a = 0\), the delay instruction is executed.

The delay instruction following a Bicc (other than BA) should not be a delayed-control-transfer instruction. The results of following a Bicc with another delayed control transfer instruction are implementation-dependent and therefore unpredictable.

**Traps:**

- none
<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Cond.</th>
<th>Operation</th>
<th>icc Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>BN</td>
<td>0000</td>
<td>Branch Never</td>
<td>No test</td>
</tr>
<tr>
<td>BE</td>
<td>0001</td>
<td>Branch on Equal</td>
<td>z</td>
</tr>
<tr>
<td>BLE</td>
<td>0010</td>
<td>Branch on Less or Equal</td>
<td>z OR (n XOR v)</td>
</tr>
<tr>
<td>BL</td>
<td>0011</td>
<td>Branch on Less</td>
<td>n XOR v</td>
</tr>
<tr>
<td>BLEU</td>
<td>0100</td>
<td>Branch on Less or Equal, Unsigned</td>
<td>c OR z</td>
</tr>
<tr>
<td>BCS</td>
<td>0101</td>
<td>Branch on Carry Set (Less than, Unsigned)</td>
<td>c</td>
</tr>
<tr>
<td>BNEG</td>
<td>0110</td>
<td>Branch on Negative</td>
<td>n</td>
</tr>
<tr>
<td>BVS</td>
<td>0111</td>
<td>Branch on oVerflow Set</td>
<td>v</td>
</tr>
<tr>
<td>BA</td>
<td>1000</td>
<td>Branch Always</td>
<td>No test</td>
</tr>
<tr>
<td>BNE</td>
<td>1001</td>
<td>Branch on Not Equal</td>
<td>not z</td>
</tr>
<tr>
<td>BG</td>
<td>1010</td>
<td>Branch on Greater</td>
<td>not(z OR (n XOR v))</td>
</tr>
<tr>
<td>BGE</td>
<td>1011</td>
<td>Branch on Greater or Equal</td>
<td>not(n XOR v)</td>
</tr>
<tr>
<td>BGU</td>
<td>1100</td>
<td>Branch on Greater, Unsigned</td>
<td>not(c OR z)</td>
</tr>
<tr>
<td>BCC</td>
<td>1101</td>
<td>Branch on Carry Clear (Greater than or Equal, Unsigned)</td>
<td>not c</td>
</tr>
<tr>
<td>BPOS</td>
<td>1110</td>
<td>Branch on Positive</td>
<td>not n</td>
</tr>
<tr>
<td>BVC</td>
<td>1111</td>
<td>Branch on oVerflow Clear</td>
<td>not v</td>
</tr>
</tbody>
</table>

Format:

```
 31 30 29 28 25 24 22 21  0
0 0 a cond. 0 1 0 disp22
```
Operation:
- $r[15] \leftarrow PC$
- PC $\leftarrow nPC$
- nPC $\leftarrow PC + (\text{disp30} \times 4)$

Assembler Syntax:
- `call label`

Description:
The CALL instruction causes a delayed, unconditional, PC-relative control transfer to the address $(PC + 4) + (\text{disp30} \times 4)$. The CALL instruction does not have an annul bit, therefore the delay slot instruction following the CALL instruction is always executed (See Section NO TAG). CALL first writes its return address (PC) into the $outs$ register, $r[15]$, and then adds 4 to the PC. The 32-bit displacement which is added to the new PC is formed by appending two low-order zeros to the 30-bit word displacement contained in the instruction. Consequently, the target address can be anywhere in the CY7C601’s user or supervisor address space.

If the instruction following a CALL uses register $r[15]$ as a source operand, hardware interlocks add a one cycle delay.

*Programming note:* a register-indirect CALL can be constructed using a JMPL instruction with $rd$ set to 15.

Traps:
- none

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>disp30</td>
<td></td>
</tr>
</tbody>
</table>
```
CBccc

**Operation:**

- If condition true then nPC $\leftarrow$ PC + (sign extnd(disp22) x 4)
- else nPC $\leftarrow$ nPC + 4

**Assembler Syntax:**

cba{,a}  
cbn{,a}  
cb3{,a}  
cb2{,a}  
cb23{,a}  
cb1{,a}  
cb13{,a}  
cb12{,a}  
cb123{,a}  
eb0{,a}  
eb03{,a}  
eb02{,a}  
eb023{,a}  
eb01{,a}  
eb013{,a}  
eb012{,a}  

**Description:**

The CBccc instructions (except for CBA and CBN) evaluate specific coprocessor condition code combinations (from the CCC<1:0> inputs) based on the branch type as specified by the value in the instruction’s `cond` field. If the specified combination of condition codes evaluates as true, the branch is taken, causing a delayed, PC-relative control transfer to the address (PC + 4) + (sign extnd(disp22) x 4). If the condition codes evaluate as false, the branch is not taken. See Section NO TAG regarding control transfer instructions.

If the branch is not taken, the annul bit field (a) is checked. If a is set, the instruction immediately following the branch instruction (the delay instruction) is not executed (i.e., it is annulled). If the annul field is zero, the delay instruction is executed. If the branch is taken, the annul field is ignored, and the delay instruction is executed. See Section NO TAG regarding delayed branching.

Branch Never (CBN) executes like a NOP, except it obeys the annul field with respect to its delay instruction.

Branch Always (CBA), because it always branches regardless of the condition codes, would normally ignore the annul field. Instead, it follows the same annul field rules: if $a=1$, the delay instruction is annulled; if $a=0$, the delay instruction is executed.

To prevent misapplication of the condition codes, a non-coprocessor instruction must immediately precede a CBccc instruction.

A CBccc instruction generates a cp_disabled trap (and does not branch or annul) if the PSR’s EC bit is reset or if no coprocessor is present.

Note: The instruction’s annul bit field, a, is set by appending “.a” after the branch name. If it is not appended, the a field is automatically reset. “.a” is shown in braces because it is optional.
### Traps:
- cp_disabled
- cp_exception

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>cond.</th>
<th>CCC&lt;1:0&gt; test</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBN</td>
<td>0000</td>
<td>Never</td>
</tr>
<tr>
<td>CB123</td>
<td>0001</td>
<td>1 or 2 or 3</td>
</tr>
<tr>
<td>CB12</td>
<td>0010</td>
<td>1 or 2</td>
</tr>
<tr>
<td>CB13</td>
<td>0011</td>
<td>1 or 3</td>
</tr>
<tr>
<td>CB1</td>
<td>0100</td>
<td>1</td>
</tr>
<tr>
<td>CB23</td>
<td>0101</td>
<td>2 or 3</td>
</tr>
<tr>
<td>CB2</td>
<td>0110</td>
<td>2</td>
</tr>
<tr>
<td>CB3</td>
<td>0111</td>
<td>3</td>
</tr>
<tr>
<td>CBA</td>
<td>1000</td>
<td>Always</td>
</tr>
<tr>
<td>CB0</td>
<td>1001</td>
<td>0</td>
</tr>
<tr>
<td>CB03</td>
<td>1010</td>
<td>0 or 3</td>
</tr>
<tr>
<td>CB02</td>
<td>1011</td>
<td>0 or 2</td>
</tr>
<tr>
<td>CB023</td>
<td>1100</td>
<td>0 or 2 or 3</td>
</tr>
<tr>
<td>CB01</td>
<td>1101</td>
<td>0 or 1</td>
</tr>
<tr>
<td>CB013</td>
<td>1110</td>
<td>0 or 1 or 3</td>
</tr>
<tr>
<td>CB012</td>
<td>1111</td>
<td>0 or 1 or 2</td>
</tr>
</tbody>
</table>

#### Format:

```plaintext
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>25</th>
<th>24</th>
<th>22</th>
<th>21</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>a</td>
<td>1</td>
<td>1</td>
<td>11</td>
<td>disp22</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
**Operation:** Dependent on Coprocessor implementation

**Assembler Syntax:** Unspecified

**Description:**

CPop1 and CPop2 are the instruction formats for coprocessor operate instructions. The \( op3 \) field for CPop1 is 110110; for CPop2 it’s 110111. The coprocessor operations themselves are encoded in the \( opc \) field and are dependent on the coprocessor implementation. Note that this does not include load/store coprocessor instructions, which fall into the integer unit’s load/store instruction category.

All CPop instructions take all operands from, and return all results to, the coprocessor’s registers. The data types supported, how the operands are aligned, and whether a CPop generates a cp_exception trap are Coprocessor dependent.

A CPop instruction causes a cp_disabled trap if the PSR’s EC bit is reset or if no coprocessor is present.

**Traps:**
- cp_disabled
- cp_exception

**Format:**

```
          rd 110110 rs1 opc rs2
01 31 30 29 25 24 19 18 14 13  5  4
          rd 110111 rs1 opc rs2
```

MATRA MHS
Rev. A (10/09/96)
FABSs

Absolute Value Single

(FPU Instruction Only)

**Operation:**
\[ f[rd] \leftarrow f[rs2] \text{ AND } 7FFFFFFF H \]

**Assembler Syntax:**
`fabss freg rs2, freg rd`

**Description:**
The FABSs instruction clears the sign bit of the word in `f[rs2]` and places the result in `f[rd]`. It does not round.

Since `rs2` can be either an even or odd register, FABSs can also operate on the high-order words of double and extended operands, which accomplishes sign bit clear for these data types.

**Traps:**
- `fp_disabled`
- `fp_exception`*

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.*
### FADDd

**Add Double**

(FPU Instruction Only)

**Operation:**

\[ f[rd]d \leftarrow f[rs1]d + f[rs2]d \]

**Assembler Syntax:**

`fadd d freg rs1, freg rs2, freg rd`

**Description:**

The FADDd instruction adds the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) to the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \) and \( f[rd+1] \).

**Traps:**

- `fp_disabled`
- `fp_exception (of, uf, nv, nx)`

**Format:**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>10</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>19</td>
<td>18</td>
</tr>
<tr>
<td>14</td>
<td>13</td>
<td></td>
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<td>14</td>
<td>13</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

- `rd`
- `rs1`
- `rs2`
FADDs

Add Single

(FPU Instruction Only)

Operation: \[ f[rd] \leftarrow f[rs1] + f[rs2] \]

Assembler Syntax: \[ fadds \ freg_{rs1}, \ freg_{rs2}, \ freg_{rd} \]

Description: The FADDs instruction adds the contents of \( f[rs1] \) to the contents of \( f[rs2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \).

Traps: \[ \text{fp\_disabled, fp\_exception (of, uf, nv, nx)} \]

Format:

```
   31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
   0  rd  1 1 0 1 0 0  \  0 0 1 0 0 0 0 0 1  \  rs2
```

FADDs
FADDx

Add Extended FADDx

(FPU Instruction Only)

Operation: $f[rd]x \leftarrow f[rs1]x + f[rs2]x$

Assembler Syntax: 
faddx freg_rs1, freg_rs2, freg_rd


Traps: fp_disabled
fp_exception (of, uf, nv, nx)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>rs1</td>
<td>001000011</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**FBfcc**

**Floating-Point Conditional Branch**

**Operation:**

PC ← nPC

If condition true then nPC ← PC + (sign extnd(disp22) x 4)
else nPC ← nPC + 4

**Assembler Syntax:**

- fba{,a}  
- fbn{,a}  
- fbu{,a}  
- fbg{,a}  
- fbug{,a}  
- fb{,a}  
- fbu{,a}  
- fbng{,a}  
- fncc{,a}  
- fbc{,a}  
- fbe{,a}  
- fbgc{,a}  
- fbcg{,a}  
- fbuge{,a}  
- fble{,a}  
- fbule{,a}  
- fbof{,a}  

**Note:** The instruction’s annul bit field, a, is set by appending “,a” after the branch name. If it is not appended, the a field is automatically reset. “,a” is shown in braces because it is optional.

**Description:**

The FBfcc instructions (except for FBA and FBN) evaluate specific floating-point condition code combinations (from the FCC<1:0> inputs) based on the branch type, as specified by the value in the instruction’s cond field. If the specified combination of condition codes evaluates as true, the branch is taken, causing a delayed, PC-relative control transfer to the address (PC + 4) + (sign extnd(disp22) x 4). If the condition codes evaluate as false, the branch is not taken. See Section NO TAG for additional information on control transfer instructions.

If the branch is not taken, the annul bit field (a) is checked. If a is set, the instruction immediately following the branch instruction (the delay instruction) is not executed (i.e., it is annulled). If the annul field is zero, the delay instruction is executed. If the branch is taken, the annul field is ignored, and the delay instruction is executed. See Section NO TAG regarding delayed branch instructions.

Branch Never (FBN) executes like a NOP, except it obeys the annul field with respect to its delay instruction.

Branch Always (FBA), because it always branches regardless of the condition codes, would normally ignore the annul field. Instead, it follows the same annul field rules: if a=1, the delay instruction is annulled; if a=0, the delay instruction is executed.

To prevent misapplication of the condition codes, a non-floating-point instruction must immediately precede an FBfcc instruction.

An FBfcc instruction generates an fp_disabled trap (and does not branch or annul) if the PSR’s EF bit is reset or if no Floating-Point Unit is present.
Traps:  
fp_disabled  
fp_exception*

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Cond.</th>
<th>Operation</th>
<th>fcc Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>FBN</td>
<td>0000</td>
<td>Branch Never</td>
<td>no test</td>
</tr>
<tr>
<td>FBNE</td>
<td>0001</td>
<td>Branch on Not Equal</td>
<td>U or L or G</td>
</tr>
<tr>
<td>FBLG</td>
<td>0010</td>
<td>Branch on Less or Greater</td>
<td>L or G</td>
</tr>
<tr>
<td>FBUL</td>
<td>0011</td>
<td>Branch on Unordered or Less</td>
<td>U or L</td>
</tr>
<tr>
<td>FBL</td>
<td>0100</td>
<td>Branch on Less</td>
<td>L</td>
</tr>
<tr>
<td>FBUG</td>
<td>0101</td>
<td>Branch on Unordered or Greater</td>
<td>U or G</td>
</tr>
<tr>
<td>FBG</td>
<td>0110</td>
<td>Branch on Greater</td>
<td>G</td>
</tr>
<tr>
<td>FBU</td>
<td>0111</td>
<td>Branch on Unordered</td>
<td>U</td>
</tr>
<tr>
<td>FBA</td>
<td>1000</td>
<td>Branch Always</td>
<td>no test</td>
</tr>
<tr>
<td>FBE</td>
<td>1001</td>
<td>Branch on Equal</td>
<td>E</td>
</tr>
<tr>
<td>FBUE</td>
<td>1010</td>
<td>Branch on Unordered or Equal</td>
<td>U or E</td>
</tr>
<tr>
<td>FBGE</td>
<td>1011</td>
<td>Branch on Greater or Equal</td>
<td>G or E</td>
</tr>
<tr>
<td>FBUGE</td>
<td>1100</td>
<td>Branch on Unordered or Greater or Equal</td>
<td>U or G or E</td>
</tr>
<tr>
<td>FBLE</td>
<td>1101</td>
<td>Branch on Less or Equal</td>
<td>L or E</td>
</tr>
<tr>
<td>FBULE</td>
<td>1110</td>
<td>Branch on Unordered or Less or Equal</td>
<td>U or L or E</td>
</tr>
<tr>
<td>FBO</td>
<td>1111</td>
<td>Branch on Ordered</td>
<td>L or G or E</td>
</tr>
</tbody>
</table>

Format:  
```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>25</th>
<th>24</th>
<th>22</th>
<th>21</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>a</td>
<td>cond.</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>disp22</td>
<td></td>
</tr>
</tbody>
</table>
```

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.*

MATRA MHS  
Rev. A (10/09/96)
FCMPd

Compare Double

(FPU Instruction Only)

Operation: \( fcc \leftarrow f[rs1]d \) COMPARE \( f[rs2]d \)

Assembler Syntax: \texttt{fcmpd}\ freg rs1, freg rs2

Description: FCMPd subtracts the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) from the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR's \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f1 = f2 )</td>
</tr>
<tr>
<td>1</td>
<td>( f1 &lt; f2 )</td>
</tr>
<tr>
<td>2</td>
<td>( f1 &gt; f2 )</td>
</tr>
<tr>
<td>3</td>
<td>( f1 \neq f2 ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f1 \) stands for the contents of \( f[rs1] \), \( f[rs1+1] \) and \( f2 \) represents the contents of \( f[rs2] \), \( f[rs2+1] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfccc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfccc instruction.

FCMPd causes an invalid exception (nv) if either operand is a signaling NaN.

Traps: fp_disabled
fp_exception (nv)

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
```
FCMPEd Compare Double and Exception if Unordered FCMPEd
(FPU Instruction Only)

Operation: \( \text{fcc} \leftarrow f[rs1]d \ \text{COMPARE} \ f[rs2]d \)

Assembler Syntax: `fcmped freg[rs1],freg[rs2]`

Description: FCMPEd subtracts the contents of \( f[rs2] \ \text{CONCAT} \ f[rs2+1] \) from the contents of \( f[rs1] \ \text{CONCAT} \ f[rs1+1] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>( fcc )</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f_{s1} = f_{s2} )</td>
</tr>
<tr>
<td>1</td>
<td>( f_{s1} &lt; f_{s2} )</td>
</tr>
<tr>
<td>2</td>
<td>( f_{s1} &gt; f_{s2} )</td>
</tr>
<tr>
<td>3</td>
<td>( f_{s1} \neq f_{s2} ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f_{s1} \) stands for the contents of \( f[rs1] \), \( f[rs1+1] \) and \( f_{s2} \) represents the contents of \( f[rs2] \), \( f[rs2+1] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPEd causes an invalid exception (nv) if either operand is a signaling or quiet NaN.

Traps: `fp_disabled`
`fp_exception (nv)`

Format:

```
  31 30 29 25 24 19 18 14 13 5 4 0
1 0 ignored 1 1 0 1 0 1 rs1 0 0 1 0 1 0 1 0 rs2
```
FCMPEs: Compare Single and Exception if Unordered FCMPEs

(FPU Instruction Only)

Operation: \[ \text{fcc} \leftarrow \text{f}[\text{rs1}] \text{ COMPARE } \text{f}[\text{rs2}] \]

Assembler Syntax: \[ \text{fcmpes } \text{freg}\text{rs1}, \text{freg}\text{rs2} \]

Description: FCMPEs subtracts the contents of \( f[\text{rs2}] \) from the contents of \( f[\text{rs1}] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( \text{fcc} \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>( \text{fcc} )</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f[\text{rs1}] = f[\text{rs2}] )</td>
</tr>
<tr>
<td>1</td>
<td>( f[\text{rs1}] &lt; f[\text{rs2}] )</td>
</tr>
<tr>
<td>2</td>
<td>( f[\text{rs1}] &gt; f[\text{rs2}] )</td>
</tr>
<tr>
<td>3</td>
<td>( f[\text{rs1}] \neq f[\text{rs2}] ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f[\text{rs1}] \) stands for the contents of \( f[\text{rs1}] \) and \( f[\text{rs2}] \) represents the contents of \( f[\text{rs2}] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBf cc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBf cc instruction.

FCMPEs causes an invalid exception (nv) if either operand is a signaling or quiet NaN.

Traps: \[ \text{fp\_disabled} \]
\[ \text{fp\_exception (nv)} \]

Format:

```
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>rs1</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>rs2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
```

In this format, the first two bits (10) indicate that the instruction is ignored. The following 13 bits (11010101) represent the register number (rs1). The last 13 bits (001010101) represent the floating-point register number (rs2).
FCMPE\textsubscript{x} Compare Extended and Exception if Unordered FCMPE

\textbf{(FPU Instruction Only)}

\textbf{Operation:} \texttt{fcc} \leftarrow f[rs1] \texttt{x} \texttt{COMPARE} f[rs2] \texttt{x}

\textbf{Assembler Syntax:} \texttt{fcmpex} \texttt{freg\_rs1}, \texttt{freg\_rs2}

\textbf{Description:} FCMPE\textsubscript{x} subtracts the contents of \texttt{f[rs2]} CONCAT \texttt{f[rs2+1]} CONCAT \texttt{f[rs2+2]} from the contents of \texttt{f[rs1]} CONCAT \texttt{f[rs1+1]} CONCAT \texttt{f[rs1+2]} following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \texttt{fcc} bits are set accordingly, and then the result is discarded. The codes are set as follows:

\begin{center}
\begin{tabular}{|c|c|}
\hline
\texttt{fcc} & \texttt{Relation} \\
\hline
0 & f_{s1} = f_{s2} \\
1 & f_{s1} < f_{s2} \\
2 & f_{s1} > f_{s2} \\
3 & f_{s1} \neq f_{s2} \text{ (unordered)} \\
\hline
\end{tabular}
\end{center}

In this table, \texttt{f}_1 stands for the contents of \texttt{f[rs1]}, \texttt{f[rs1+1]}, \texttt{f[rs1+2]} and \texttt{f}_2 represents the contents of \texttt{f[rs2]}, \texttt{f[rs2+1]}, \texttt{f[rs2+2]}.

Compare instructions are used to set up the floating-point condition codes for a subsequent FB\texttt{fcc} instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FB\texttt{fcc} instruction.

FCMPE\textsubscript{x} causes an invalid exception (nv) if either operand is a signaling or quiet NaN.

\textbf{Traps:}
\begin{itemize}
  \item fp\_disabled
  \item fp\_exception (nv)
\end{itemize}

\textbf{Format:}

\begin{center}
\begin{tabular}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 5 & 4 & 0 \\
\hline
1 & 0 & ignored & 1 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & rs2
\end{tabular}
\end{center}
FCMPs

(FPU Instruction Only)

Operation: \( \text{fcc} \leftarrow \text{f}[\text{rs1}] \) COMPARE \( \text{f}[\text{rs2}] \)

Assembler Syntax: \text{fcmps } freg_{rs1} , freg_{rs2}

Description: FCMPs subtracts the contents of \( f[rs2] \) from the contents of \( f[rs1] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f[rs1] = f[rs2] )</td>
</tr>
<tr>
<td>1</td>
<td>( f[rs1] &lt; f[rs2] )</td>
</tr>
<tr>
<td>2</td>
<td>( f[rs1] &gt; f[rs2] )</td>
</tr>
<tr>
<td>3</td>
<td>( f[rs1] \neq f[rs2] ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f[rs1] \) stands for the contents of \( f[rs1] \) and \( f[rs2] \) represents the contents of \( f[rs2] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBf:cc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBf:cc instruction.

FCMPs causes an invalid exception (nv) if either operand is a signaling NaN.

Traps: fp_disabled fp_exception (nv)

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 17 & 16 & 15 & 14 & 13 & 5 & 4 & 0 \\
1 & 0 & \text{ignored} & 1 & 1 & 0 & 1 & 0 & 1 & rs1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & rs2
\end{array}
\]
FCMPx
(FPU Instruction Only)

Operation: \( fcc \leftarrow f[r_s1]x \) COMPARE \( f[r_s2]x \)

Assembler Syntax: \( \text{fcmpx} \ freg_{rs1}, freg_{rs2} \)

Description: FCMPx subtracts the contents of \( f[r_s2] \) CONCAT \( f[r_s2+1] \) CONCAT \( f[r_s2+2] \) from the contents of \( f[r_s1] \) CONCAT \( f[r_s1+1] \) CONCAT \( f[r_s1+2] \) following the ANSI/IEEE 754-1985 standard. The result is evaluated, the FSR’s \( fcc \) bits are set accordingly, and then the result is discarded. The codes are set as follows:

<table>
<thead>
<tr>
<th>fcc</th>
<th>Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( f_s1 = f_s2 )</td>
</tr>
<tr>
<td>1</td>
<td>( f_s1 &lt; f_s2 )</td>
</tr>
<tr>
<td>2</td>
<td>( f_s1 &gt; f_s2 )</td>
</tr>
<tr>
<td>3</td>
<td>( f_s1 \neq f_s2 ) (unordered)</td>
</tr>
</tbody>
</table>

In this table, \( f_s1 \) stands for the contents of \( f[r_s1] \), \( f[r_s1+1] \), \( f[r_s1+2] \) and \( f_s2 \) represents the contents of \( f[r_s2] \), \( f[r_s2+1] \), \( f[r_s2+2] \).

Compare instructions are used to set up the floating-point condition codes for a subsequent FBfcc instruction. However, to prevent misapplication of the condition codes, at least one non-floating-point instruction must be executed between an FCMP and a subsequent FBfcc instruction.

FCMPx causes an invalid exception (nv) if either operand is a signaling NaN.

Traps: fp-disabled
fp_exception (nv)

Format:

```
  31  30  29  28  27  26  25  24  19  18  14  13  5  4  0
  1  0  ignored 1 1 0 1 0 1  rs1  0 0 1 0 1 0 0 1 1  rs2
```
FDIVd  Divide Double  FDIVd
(FPU Instruction Only)

Operation:  \( f[rd]d \leftarrow f[rs1]d / f[rs2]d \)

Assembler Syntax:  \( fdivd \ freg_{rs1}, \ freg_{rs2}, \ freg_{rd} \)

Description:  The FDIVd instruction divides the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) by the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \) and \( f[rd+1] \).

Traps:  \( fp\_disabled \)
\( fp\_exception \) (of, uf, dz, nv, nx)

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>
```
FDIVs  

Divide Single

(FPU Instruction Only)

Operation: $f[rd]s \leftarrow f[rs1]s / f[rs2]s$

Assembler Syntax: `fdifs freg rs1, freg rs2, freg rd`

Description: The FDIVs instruction divides the contents of $f[rs1]$ by the contents of $f[rs2]$ as specified by the ANSI/IEEE 754-1985 standard and places the results in $f[rd]$.

Traps: 
- `fp_disabled`
- `fp_exception (of, uf, dz, nv, nx)`

Format:

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 1  | 0  |
```
FDIVx
(FPU Instruction Only)

Operation:
f[rd]x ← f[rs1]x / f[rs2]x

Assembler Syntax:
fdivx freg_{rs1}, freg_{rs2}, freg_{rd}

Description:
The FDIVx instruction divides the contents of f[rs1] CONCAT f[rs1+1] CONCAT f[rs1+2] by the contents of f[rs2] CONCAT f[rs2+1] CONCAT f[rs2+2] as specified by the ANSI/IEEE 754-1985 standard and places the results in f[rd], f[rd+1], and f[rd+2].

Traps:
fp_disabled
fp_exception (of, uf, dz, nv, nx)

Format:

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<td>0</td>
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<td>1</td>
<td>1</td>
<td>1</td>
</tr>
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<td></td>
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<td>rs2</td>
</tr>
</tbody>
</table>
```
FdTOi
Convert Double to Integer
(FPU Instruction Only)

Operation: $f[rd] \leftarrow f[rs2]d$

Assembler Syntax: `fdtoi freg `frs2`, freg `rd`

Description: FdTOi converts the floating-point double contents of $f[rs2]$ CONCAT $f[rs2+1]$ to a 32-bit, signed integer by rounding toward zero as specified by the ANSI/IEEE 754-1985 standard. The result is placed in $f[rd]$. The rounding direction field ($RD$) of the FSR is ignored.

Traps: `fp_disabled`
`fp_exception (nv, nx)`

Format:

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<td>rd</td>
<td>11</td>
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<td>ignored</td>
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<td>10</td>
<td>0</td>
<td>10</td>
<td>0</td>
<td>10</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>
FdTOs
Convert Double to Single
(FPU Instruction Only)

Operation:  \( f[rd] \leftarrow f[rs2]d \)

Assembler Syntax:  \( fdtos \ freg_{rs2} \ freg_{rd} \)

Description:  FdTOs converts the floating-point double contents of \( f[rs2] \) \( \text{CONCAT} \) \( f[rs2+1] \) to a single-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). Rounding is performed according to the rounding direction field (\( RD \)) of the FSR.

Traps:  \( \text{fp\_disabled} \)
\( \text{fp\_exception (of, uf, nv, nx)} \)

Format:

```
  31  30  29  28  27  26  25  24  19 18  14 13  5  4  0
  1  0  rd  1  1  0  1  0  0  ignored  0  1  1  0  0  1  1  0  rs2
```
FdTOx  Convert Double to Extended  FdTOx
(FPU Instruction Only)

Operation:  \( f[rd] \leftarrow f[rs2]d \)

Assembler Syntax:  \( \text{fdtox} \ freg\_rs2, \ freg\_rd \)

Description:  FdTOx converts the floating-point double contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) to an extended-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \). Rounding is performed according to the rounding direction (RD) and rounding precision (RP) fields of the FSR.

Traps:  fp_disabled
fp_exception (nv)

Format:

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<tr>
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<td>rd</td>
<td>1 1 0 1 0 0</td>
<td>ignored</td>
<td>0 1 1 0 0 1 1 1 0</td>
<td>rs2</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
FiTOd  Convert Integer to Double  FiTOd
(FPU Instruction Only)

Operation:  \( f[rd] \leftarrow f[rs2] \)

Assembler Syntax:  \( \text{fitod} \ freg_{rs2} , freg_{rd} \)

Description: FiTOd converts the 32-bit, signed integer contents of \( f[rs2] \) to a floating-point, double-precision format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \) and \( f[rd+1] \).

Traps:  \( \text{fp_disabled} \)
\( \text{fp_exception}^* \)

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 1  | 1  | 0 | 1 | 0 | 0 | ignored | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | rs2 |

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
FiTOs  Convert Integer to Single  FiTOs
(FPU Instruction Only)

Operation:  \( f[rd] \leftarrow f[rs2] \)

Assembler Syntax:  \texttt{fitos} \texttt{ freg }_{rs2} , \texttt{freg}_{rd} 

Description:  FiTOs converts the 32-bit, signed integer contents of \( f[rs2] \) to a floating-point, single-precision format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). Rounding is performed according to the rounding direction field, \( RD \).

Traps:  \texttt{fp\_disabled}  \\
\texttt{fp\_exception (nx)}

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 5 & 4 & 0 \\
1 & 0 & rd & 110100 & ignored & 011000100 & rs2
\end{array}
\]
FiTOx  Convert Integer to Extended  FiTOx
(FPU Instruction Only)

Operation:  \( f[rd] \leftarrow f[rs2] \)

Assembler Syntax:  

\[
\text{fitox } freg_{rs2} . freg_{rd}
\]

Description:  FiTOx converts the 32-bit, signed integer contents of \( f[rs2] \) to an extended-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \).

Traps:  
- \( \text{fp\_disabled} \)
- \( \text{fp\_exception}^* \)

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  |    |    | 1  | 1  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | rs2 |

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
FMOVs

Move FMOVs

(FPU Instruction Only)

Operation: \( f[rd] \leftarrow f[rs2] \)

Assembler Syntax: \( \text{fmovs } f_{reg2}, f_{reg1d} \)

Description: The FMOVs instruction moves the word content of register \( f[rs2] \) to the register \( f[rd] \). Multiple FMOVs’s are required to transfer multiple-precision numbers between \( f \) registers.

Traps: \( \text{fp}_\text{disabled} \)
\( \text{fp}_\text{exception}^* \)

Format:

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<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>ignored</td>
<td>00000001</td>
<td>rs2</td>
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</tbody>
</table>

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
## FMULd

### Multiply Double

*(FPU Instruction Only)*

**Operation:**
\[ f[rd] \leftarrow f[rs1]d \times f[rs2]d \]

**Assembler Syntax:**
```
fmuld freg rs1, freg rs2, freg rd
```

**Description:**
The FMULd instruction multiplies the contents of \( f[rs1] \) CONCAT \( f[rs1+1] \) by the contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \) and \( f[rd+1] \).

**Traps:**
- fp_disabled
- fp_exception (of, uf, nv, nx)

**Format:**

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<td>18</td>
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<td>13</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>110100</td>
<td>rs1</td>
<td>001001010</td>
<td>rs2</td>
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</tr>
</tbody>
</table>

*MATRA MHS*

Rev. A (10/09/96)
FMULs  Multiply Single  FMULs
(FPU Instruction Only)

Operation:  \( f\{rd\} \leftarrow f\{rs1\} \times f\{rs2\} \)

Assembler Syntax:  \texttt{fmuls freg\_rs1, freg\_rs2, freg\_rd}  

Description:  The FMULs instruction multiplies the contents of \( f\{rs1\} \) by the contents of \( f\{rs2\} \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f\{rd\} \).

Traps:  \texttt{fp\_disabled}  
\texttt{fp\_exception (of, uf, nv, nx)}

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| \( 1 \) | \( 0 \) | \( rd \) | 110100 | \( rs1 \) | 001001001 | \( rs2 \) |
FMULx

Multiply Extended

(FPU Instruction Only)

Operation:  \( f[\text{rd}]x \leftarrow f[\text{rs1}]x \times f[\text{rs2}]x \)

Assembler Syntax:  \text{fmulx } f\text{reg }_r, f\text{reg }_s, f\text{reg }_d \\

Description:  The FMULx instruction multiplies the contents of \( f[\text{rs1}] \) CONCAT \( f[\text{rs1}+1] \) CONCAT \( f[\text{rs1}+2] \) by the contents of \( f[\text{rs2}] \) CONCAT \( f[\text{rs2}+1] \) CONCAT \( f[\text{rs2}+2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[\text{rd}], f[\text{rd}+1], \) and \( f[\text{rd}+2] \).

Traps:  \text{fp\_disabled, \text{fp\_exception (of, uf, nv, nx)}}

Format:

\[
\begin{array}{cccccccc}
1 & 0 & \text{rd} & 1 & 1 & 0 & 1 & 0 & 0 & \text{rs1} & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 & \text{rs2}
\end{array}
\]
FNEGs

Negate FNEGs

(FPU Instruction Only)

Operation: \[ f[rd] \leftarrow f[rs2] \text{ XOR } 80000000 \]

Assembler Syntax: \text{fnegs \_} freg_{rs2}, freg_{rd}

Description: The FNEGs instruction complements the sign bit of the word in \( f[rs2] \) and places the result in \( f[rd] \). It does not round.

Since this FPop can address both even and odd \( f \) registers, FNEGs can also operate on the high-order words of double and extended operands, which accomplishes sign bit negation for these data types.

Traps: \text{fp\_disabled, fp\_exception*}

Format:

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<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>rd</td>
<td>11</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
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</tbody>
</table>

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
FSQRTd
Square Root Double
(FPU Instruction Only)

Operation:  \( f[rd]d \leftarrow \text{SQRT } f[rs2]d \)

Assembler Syntax:  \( \text{fsqrtd } freg_{rs2}, freg_{rd} \)

Description:  FSQRTd generates the square root of the floating-point double contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \) and \( f[rd+1] \). Rounding is performed according to the rounding direction field (\( RD \)) of the FSR.

Traps:  \( fp\_disabled \)
\( fp\_exception (nv, nx) \)

Format:

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<td>1</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>0</td>
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</tr>
</tbody>
</table>

Notes:
- \( f \): Floating-point register
- \( rs2 \): Register specifier
- \( rd \): Result destination register
- \( RD \): Rounding direction field
FSQRTs
Square Root Single
(FPU Instruction Only)

Operation: \( f[rd] \leftarrow \text{SQRT} f[rs2] \)

Assembler Syntax: `fsqrts freg, freg`

Description: FSQRTs generates the square root of the floating-point single contents of \( f[rs2] \) as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). Rounding is performed according to the rounding direction field (RD) of the FSR.

Traps: `fp_disabled`, `fp_exception (nv, nx)`

Format:

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<td>1</td>
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<td>rd</td>
<td>11</td>
<td>01</td>
<td>0</td>
<td>ignored</td>
<td>00</td>
</tr>
</tbody>
</table>
```
FSQRTx

Square Root Extended
(FPU Instruction Only)

Operation:
\( f[rd]x \leftarrow \text{SQRT} f[rs2]x \)

Assembler Syntax:
\[ \text{fsqrtx freg}_{rs2}, \text{freg}_{rd} \]

Description:
FSQRTx generates the square root of the floating-point extended contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \), \( f[rd+1] \), and \( f[rd+2] \). Rounding is performed according to the rounding direction (\( RD \)) and rounding precision (\( RP \)) fields of the FSR.

Traps:
- \( \text{fp_disabled} \)
- \( \text{fp_exception (nv, nx)} \)

Format:

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</table>

\( rs2 \)
**FsTOd**  
Convert Single to Double  
*(FPU Instruction Only)*

**Operation:**  
f\[rd\]d $\leftarrow$ f\[rs2\]s

**Assembler Syntax:**  
`fstod freg\[rs2\], freg\[rd\]`

**Description:**  
FsTOd converts the floating-point single contents of f\[rs2\] to a double-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in f\[rd\] and f\[rd+1\]. Rounding is performed according to the rounding direction field (RD) of the FSR.

**Traps:**  
- fp_disabled
- fp_exception (nv)

**Format:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 11 | 0 | 1 | 0 | 0 | ignored | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | rs2 |

MATRA MHS  
Rev. A (10/09/96)
FsTOi  
Convert Single to Integer  
(FPU Instruction Only)

**Operation:**  
f[rd] ← f[rs2]

**Assembler Syntax:**  
`fstoi reg rs2, reg rd`

**Description:**  
FsTOi converts the floating-point single contents of f[rs2] to a 32-bit, signed integer by rounding toward zero as specified by the ANSI/IEEE 754-1985 standard. The result is placed in f[rd]. The rounding field (RD) of the FSR is ignored.

**Traps:**  
`fp_disabled`
`fp_exception (nv, nx)`

**Format:**

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<th>15</th>
<th>14</th>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0</td>
<td>rd</td>
<td>1 1 0 1 0 0</td>
<td>ignored</td>
<td>0 1 1 0 1 0 0 0 1</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
FsTOx  
Convert Single to Extended  
(FPU Instruction Only)

Operation:  
f[rd]x ← f[rs2]s

Assembler Syntax:  
fstox freg rs2, freg rd

Description:  
FsTOx converts the floating-point single contents of f[rs2] to an extended-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in f[rd], f[rd+1], and f[rd+2]. Rounding is performed according to the rounding direction (RD) and rounding precision (RP) fields of the FSR.

Traps:  
fp_disabled
fp_exception (nv)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>11</td>
<td>10</td>
<td>0</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
FSUBd

Subtract Double

(FPU Instruction Only)

Operation:  \( f[r_d]d \leftarrow f[r_s1]d - f[r_s2]d \)

Assembler Syntax:  \texttt{fsubd \_freg\_rs1, \_freg\_rs2, \_freg\_rd}  

Description:  The FSUBd instruction subtracts the contents of \( f[r_s2] \) CONCAT \( f[r_s2+1] \) from the contents of \( f[r_s1] \) CONCAT \( f[r_s1+1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[r_d] \) and \( f[r_d+1] \).

Traps:  \texttt{fp\_disabled}  
\texttt{fp\_exception (of, uf, nx, nv)}

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    | 1  | 0  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    | rd | 1  | 1 | 0 | 1 | 0 | 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    | rs1|    |    | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
FSUBs

Subtract Single

(FPU Instruction Only)

Operation:
\[ f[rd] \leftarrow f[rs1] - f[rs2] \]

Assembler Syntax:
`fsubs freg rs1, freg rs2, freg rd`

Description:
The FSUBs instruction subtracts the contents of \( f[rs2] \) from the contents of \( f[rs1] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd] \).

Traps:
- `fp_disabled`
- `fp_exception (of, uf, nx, nv)`

Format:

```
  31 30 29 25 24 19 18 14 13  5  4  0
  1 0  rd  11 0 1 0 0  rs1  0 0 1 0 0 0 1 0 1  rs2
```
FSUBx
Subtract Extended
(FPU Instruction Only)

Operation:
\[ f[rd]x \leftarrow f[rs1]x - f[rs2]x \]

Assembler Syntax:
\texttt{fsubx freg}_{rs1}, freg}_{rs2}, freg}_{rd}

Description:
The FSUBx instruction subtracts the contents of \( f[rs2] \text{ CONCAT } f[rs2+1] \text{ CONCAT } f[rs2+2] \) from the contents of \( f[rs1] \text{ CONCAT } f[rs1+1] \text{ CONCAT } f[rs1+2] \) as specified by the ANSI/IEEE 754-1985 standard and places the results in \( f[rd], f[rd+1], \text{ and } f[rd+2] \).

Traps:
- fp\_disabled
- fp\_exception (of, uf, nv, nx)

Format:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | 09 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 11 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | rs1| 00 | 1 | 0 | 0 | 1 | 1 | 1 | rs2|
FxTOd
Convert Extended to Double
(FPU Instruction Only)

Operation: \( f[\text{rd}] \leftarrow f[\text{rs2}] \times \)

Assembler Syntax: `fxtod freg_rs2, freg_rd`

Description: FxTOd converts the floating-point extended contents of \( f[\text{rs2}] \) CONCAT \( f[\text{rs2+1}] \) CONCAT \( f[\text{rs2+2}] \) to a double-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[\text{rd}] \) and \( f[\text{rd+1}] \). Rounding is performed according to the rounding direction (RD) field of the FSR.

Traps: `fp_disabled`
`fp_exception (of, uf, nv, nx)`

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ignored</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
```
FxTOi

Convert Extended to Integer

(FPU Instruction Only)

Operation: \( f[r_d]i \leftarrow f[r_{s2}]x \)

Assembler Syntax: \( \text{fxtoi } f_{\text{reg}rs2},f_{\text{reg}rd} \)

Description: FxTOi converts the floating-point extended contents of \( f[rs2] \) CONCAT \( f[rs2+1] \) CONCAT \( f[rs2+2] \) to a 32-bit, signed integer by rounding toward zero as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \( f[rd] \). The rounding field (\( RD \)) of the FSR is ignored.

Traps: \( \text{fp\_disabled} \)
\( \text{fp\_exception (nv, nx)} \)

Format:

\[
\begin{array}{cccccccc}
\text{31} & \text{30} & \text{29} & \text{28} & \text{27} & \text{26} & \text{25} & \text{24} & \text{19} & \text{18} & \text{14} & \text{13} & \text{5} & \text{4} & \text{0} \\
1 & 0 & \text{rd} & 1 & 1 & 0 & 1 & 0 & 0 & \text{ignored} & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 1 & \text{rs2}
\end{array}
\]
FxTOs  Convert Extended to Single  FxTOs
(FPU Instruction Only)

Operation:  \[ f[rd] \leftarrow f[rs2] \times \]

Assembler Syntax:  \[ fxtos \_freg\_rs2, \_freg\_rd \]

Description:  FxTOs converts the floating-point extended contents of \([f[rs2] \text{ CONCAT } f[rs2+1] \text{ CONCAT } f[rs2+2]]\) to a single-precision, floating-point format as specified by the ANSI/IEEE 754-1985 standard. The result is placed in \([f[rd]]\). Rounding is performed according to the rounding direction (RD) field of the FSR.

Traps:  \[ \text{fp\_disabled} \]
\[ \text{fp\_exception (of, uf, nv, nx)} \]

Format:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>rd</td>
<td>0</td>
</tr>
<tr>
<td>18</td>
<td>1</td>
</tr>
<tr>
<td>19</td>
<td>1</td>
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<tr>
<td>20</td>
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<td>21</td>
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<td>22</td>
<td>0</td>
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<td>25</td>
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<tr>
<td>28</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>1</td>
</tr>
<tr>
<td>31</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ f[rd] \quad f[rs2] \]
**IFLUSH**  
**Instruction Cache Flush**

**Operation:**  
\[
\text{FLUSH} \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}]
\]

**Assembler Syntax:**  
\[
\text{iflush}\ address
\]

**Description:**  
The IFLUSH instruction causes a word to be flushed from an instruction cache which may be internal to the processor. The word to be flushed is at the address specified by the contents of \(r[rs1]\) plus either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one.

Since there is no internal instruction cache in the current CY7C600 family, the result of executing an IFLUSH instruction is dependent on the state of the input signal, Instruction Cache Flush Trap (IFT). If \(IFT = 1\), IFLUSH executes as a NOP, with no side effects. If \(IFT = 0\), execution of IFLUSH causes an illegal_instruction trap.

**Traps:**  
illegal_instruction

**Format:**

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>25</td>
<td>24</td>
<td>19</td>
<td>18</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>ignored</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
**JMPL**

**Jump and Link**

**JMPL**

**Operation:**

\[ r[rd] \rightarrow PC \]

\[ PC \leftarrow nPC \]

\[ nPC \leftarrow r[rs1] + (r[rs2] or sign extnd(simm13)) \]

**Assembler Syntax:**

\[ jmpl \quad \text{address, reg rd} \]

**Description:**

JMPL first provides linkage by saving its return address into the register specified in the \(rd\) field. It then causes a register-indirect, delayed control transfer to an address specified by the sum of the contents of \(r[rs1]\) and either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one.

If either of the low-order two bits of the jump address is nonzero, a memory_address_not_aligned trap is generated.

**Programming note:** A register-indirect CALL can be constructed using a JMPL instruction with \(rd\) set to 15. JMPL can also be used to return from a CALL. In this case, \(rd\) is set to 0 and the return (jump) address would be equal to \(r[31] + 8\).

**Traps:**

memory_address_not_aligned

**Format:**

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1110000</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1110000</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
LD Load Word

Operation: \[ r[rd] \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \]

Assembler Syntax: \[ \text{ld \ [address], \ reg}_rd \]

Description: The LD instruction moves a word from memory into the destination register, \( r[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If LD takes a trap, the contents of the destination register remain unchanged.
If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps: memory_address_not_aligned
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>simm13</td>
</tr>
</tbody>
</table>

MATRA MHS
Rev. A (10/09/96)
LDA Load Word from Alternate space

(Privileged Instruction)

Operation:
address space ← asi

r[rd] ← [r[rs1] + r[rs2]]

Assembler Syntax:
lda [regaddr] asi, reg rd

Description:
The LDA instruction moves a word from memory into the destination register, r[rd]. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2].

If LDA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

Traps:

illegal_instruction (if i=1)
privileged_instruction (if S=0)
memory_address_not_aligned
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>8</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
LDC

Load Coprocessor register

**Operation:**

\[
c[r] \leftarrow [r[r_{s1}] + (r[r_{s2}] \text{ or sign extnd(simm13))}]
\]

**Assembler Syntax:**

\[ ld \ [address], creg \text{rd} \]

**Description:**

The LDC instruction moves a word from memory into a coprocessor register, \( c[r] \). The effective memory address is derived by summing the contents of \( r[r_{s1}] \) and either the contents of \( r[r_{s2}] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If LDC takes a trap, the state of the coprocessor depends on the particular implementation.

If the instruction following a coprocessor load uses the load’s \( c[r] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

*Programming note:* If \( r_{s1} \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**

- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

**Format:**

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 17 & 16 & 15 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & rd & 1 & 1 & 0 & 0 & 0 & 0 & rs1 & \text{==0} & \text{ignored} & rs2
\end{array}
\]

\[
\begin{array}{cccccccc}
1 & 1 & rd & 1 & 1 & 0 & 0 & 0 & 0 & rs1 & \text{==1} & \text{simm13}
\end{array}
\]
**LDCSR Load Coprocessor State Register**

**Operation:** CSR ← [r[rs1] + (r[rs2] or sign extnd(simm13))]

**Assembler Syntax:**

```
ld [address], %csr
```

**Description:**

The LDCSR instruction moves a word from memory into the Coprocessor State Register. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If LDCSR takes a trap, the state of the coprocessor depends on the particular implementation.

If the instruction following a LDCSR uses the CSR as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon implementation of the coprocessor.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**

- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

**Format:**

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
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<tbody>
<tr>
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<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
LDD  Load Doubleword  LDD

Operation:

\[ r[rd] \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \]
\[ r[rd + 1] \leftarrow [(r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}) + 4] \]

Assembler Syntax:

\text{ldd [address], reg} rd

Description:
The LDD instruction moves a doubleword from memory into a destination register pair, \( r[rd] \) and \( r[rd+1] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If a data_access_exception trap takes place during the effective address memory access, the destination registers remain unchanged.

If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem. For an LDD, this applies to both destination registers.

\textit{Programming note:} If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:

memory_address_not_aligned

data_access_exception

Format:

\begin{center}
\begin{tabular}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & rd & 0 & 0 & 0 & 0 & 1 & 1 & rs1 & \( i=0 \) & ignored & rs2 \\
1 & 1 & rd & 0 & 0 & 0 & 0 & 1 & 1 & rs1 & \( i=1 \) & simm13 \\
\end{tabular}
\end{center}
LDDA
Load Doubleword from Alternate space

(Privileged Instruction)

Operation:
address space ↔ asi
r[rd] ← [r[rs1] + r[rs2]]

r[rd +1] ← [r[rs1] + r[rs2] + 4]

Assembler Syntax:
ldda [regaddr] asi, reg rd

Description:
The LDDA instruction moves a doubleword from memory into the destination registers, r[rd] and
r[rd+1]. The effective memory address is a combination of the address space value given in the asi
field and the address derived by summing the contents of r[rs1] and r[rs2]. The most significant
memory word is always moved into the even-numbered destination register and the least significant
memory word is always moved into the next odd-numbered register (see discussion in Section
NO TAG).

If a trap takes place during the effective address memory access, the destination registers re-
main unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand,
hardware interlocks add one or more delay cycles to the following instruction depending upon
the memory subsystem. For an LDDA, this applies to both destination registers.

Traps:
illegal_instruction (if i=1)
privileged_instruction (if S=0)
memory_address_not_aligned
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
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<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td>rs1</td>
<td></td>
<td>i=0</td>
<td>asi</td>
<td></td>
<td>rs2</td>
</tr>
</tbody>
</table>
LDDC
Load Doubleword Coprocessor

Operation:
\[ r[rd] \leftarrow (r[rs1] + (r[rs2] \text{ or sign extnd(simm13)})) \]
\[ r[rd+1] \leftarrow ((r[rs1] + (r[rs2] \text{ or sign extnd(simm13)})) + 4) \]

Assembler Syntax:
\text{ldd} \ [address], \ creg_{rd}

Description:
The LDDC instruction moves a doubleword from memory into the coprocessor registers, c[rd] and c[rd+1]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If LDDC takes a trap, the state of the coprocessor depends on the particular implementation.

If the instruction following a coprocessor load uses the load’s c[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem and coprocessor implementation. For an LDDC, this applies to both destination registers.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:
cp_disabled
memory_address_not_aligned
data_access_exception

Format:

<table>
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<tr>
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<th>29</th>
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<th>24</th>
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<th>12</th>
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<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>(rd)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>(rs1)</td>
<td>(i=0)</td>
<td>ignored</td>
<td>(rs2)</td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>18</th>
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<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>(rd)</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>(rs1)</td>
<td>(i=1)</td>
</tr>
</tbody>
</table>
LDDF Load Doubleword Floating-Point

Operation:
\[ f[rd] \leftarrow [r[rs1] + \left( r[rs2] \text{ or sign extnd(simm13)} \right) ] \]
\[ f[rd + 1] \leftarrow [(r[rs1] + \left( r[rs2] \text{ or sign extnd(simm13)} \right)) + 4] \]

Assembler Syntax:
\[ \text{ldd [address], freg} \]

Description:
The LDDF instruction moves a doubleword from memory into the floating-point registers, \( f[rd] \) and \( f[rd+1] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The most significant memory word is always moved into the even-numbered destination register and the least significant memory word is always moved into the next odd-numbered register (see discussion in Section NO TAG).

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If a trap takes place during the effective address memory access, the destination registers remain unchanged.

If the instruction following a floating-point load uses the load’s \( f[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem. For an LDDF, this applies to both destination registers.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:
- fp_disabled
- fp_exception*
- memory_address_not_aligned
- data_access_exception

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>18</th>
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<td>1 0 0 0 1 1</td>
<td>rs1</td>
<td>i=0</td>
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<td>rs2</td>
<td></td>
<td></td>
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</table>
```

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<table>
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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1 0 0 0 1 1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
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</tr>
</tbody>
</table>
```

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
LDF Load Floating-Point register

Operation:  \[ f[rd] \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \]

Assembler Syntax:  \text{ld} \ [\text{address}], freg \_rd

Description:  The LDF instruction moves a word from memory into a floating-point register, \( f[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction's \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If the PSR's EF bit is set to zero or if no Floating-Point Unit is present, an \text{fpDisabled} trap will be generated. If LDF takes a trap, the contents of the destination register remain unchanged.

If the instruction following a floating-point load uses the load's \( f[rd] \) register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

\textit{Programming note:} If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:  \text{fpDisabled}
\text{fpException*}
\text{memoryAddressNotAligned}
\text{dataAccessException}

Format:

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<tr>
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<th>24</th>
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<th>18</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>100000</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
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<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>100000</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
**LDFSR**  
Load Floating-Point State Register

**Operation:**  
F SR ← [r[rs1] + (r[rs2] or sign extnd(simm13))]

**Assembler Syntax:**  
`ld [address], %fsr`

**Description:**  
The LDFSR instruction moves a word from memory into the floating-point state register. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. This instruction will wait for all pending FPops to complete execution before it loads the memory word into the FSR.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If LDFSR takes a trap, the contents of the FSR remain unchanged.

If the instruction following a LDFSR uses the FSR as a source operand, hardware interlocks add one or more cycle delay to the following instruction depending upon the memory sub-system.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**  
- fp_disabled
- fp_exception*  
- memory_address_not_aligned
- data_access_exception

**Format:**

```
  31 30 29 25 24 19 18 14 13 12  5 4 0
  1 1 rd   1 0 0 0 0 1   rs1   i=0 ignored   rs2
```

```
  31 30 29 25 24 19 18 14 13 12  0
  1 1 rd   1 0 0 0 0 1   rs1   i=1 simm13
```

*NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.*
LDSB Load Signed Byte

Operation: \[ r[rd] \leftarrow \text{sign extnd}(r[rs1] + (r[rs2] \text{ or sign extnd(simm13)})) \]

Assembler Syntax: ldsb [address], reg,rd

Description: The LDSB instruction moves a signed byte from memory into the destination register, r[rd]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The fetched byte is right-justified and sign-extended in r[rd].

If LDSB takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles to the following instruction depending upon the memory subsystem.

Programmer note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps: data_access_exception

Format:

```
   31  30  29  25  24  19  18  14  13  12  5  4  0
   1  1  rd  0 0 1 0 0 1  |  rs1  | i=0  | ignored | rs2

   31  30  29  25  24  19  18  14  13  12  0
   1  1  rd  0 0 1 0 0 1  |  rs1  | i=1  | simm13
```
LDSBA  Load Signed Byte from Alternate space  LDSBA
(Privileged Instruction)

Operation:  
address space ➔ asi
r[rd] ➔ sign extnd[r[rs1] + r[rs2]]

Assembler Syntax:  
ldsba [regaddr] asi, reg rd

Description:  
The LDSBA instruction moves a signed byte from memory into the destination register, r[rd]. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2]. The fetched byte is right-justified and sign-extended in r[rd].

If LDSBA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Traps:  
illegal_instruction (if i=1)
privileged_instruction (if S=0)
data_access_exception

Format:  

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>18</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
</tr>
</tbody>
</table>
LDSH  Load Signed Halfword  LDSH

Operation:  \( r[rd] \leftarrow \text{sign extnd}[r[rs1] + (r[rs2] \text{ or sign extnd(sim13))}] \)

Assembler Syntax:  \text{ldsh} [address], reg\_rd

Description:  The LDSH instruction moves a signed halfword from memory into the destination register, \( r[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction's \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched halfword is right-justified and sign-extended in \( r[rd] \).

If LDSH takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load's \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Programming note:  If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:  memory\_address\_not\_aligned

data\_access\_exception

Format:

\[
\begin{array}{|c|c|c|c|c|c|c|c|c|c|}
\hline
31 & 30 & 29 & 28 & 27 & 26 & 25 & 19 & 18 & 14 \ 13 \ \ \\
\hline
1 & 1 & \text{rd} & 0 & 0 & 1 & 0 & 1 & 0 & \text{rs1} \ 1=0 \ \ \\
\hline
\hline
31 & 30 & 29 & 28 & 27 & 26 & 25 & 19 & 18 & 14 \ 13 \ \ \\
\hline
1 & 1 & \text{rd} & 0 & 0 & 1 & 0 & 1 & 0 & \text{rs1} \ \text{i=1} \ \ \\
\hline
\end{array}
\]

\begin{array}{|c|c|c|c|c|c|c|c|c|c|}
\hline
1 & 1 & \text{rs2} & \text{ignored} & \text{rs1} & \text{i=0} \ \ \\
\hline
1 & 1 & \text{sim13} & \text{rs1} & \text{i=1} \ \ \\
\hline
\end{array}
LDSA

Load Signed Halfword from Alternate space

(Privileged Instruction)

Operation:
address space ← asi
r[rd] ← sign extnd[r[rs1] + r[rs2]]

Assembler Syntax:
ldsha [reg addr] asi, reg rd

Description:
The LDSHA instruction moves a signed halfword from memory into the destination register, r[rd].
The effective memory address is a combination of the address space value given in the asi field and
the address derived by summing the contents of r[rs1] and r[rs2]. The fetched halfword is right-justi-
fied and sign-extended in r[rd].

If LDSHA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand,
hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Traps:
illegal_instruction (if i=1)
privileged_instruction (if S=0)
memory_address_not_aligned
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>24</th>
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<td>1</td>
<td>rd</td>
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<td>1</td>
<td>0</td>
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<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

MATRA MHS
Rev. A (10/09/96)
LDSTUB: Atomic Load/Store Unsigned Byte

**Operation:**
\[ r[rd] \leftarrow \text{zero extnd}[r[rs1] + (r[rs2] \text{ or sign extnd}(\text{simm13}))] \]
\[ \text{or} \]
\[ r[rs1] + (r[rs2] \text{ or sign extnd}(\text{simm13})) \leftarrow \text{FFFFFFFF H} \]

**Assembler Syntax:**
\[ \text{ldstub } [ \text{address} ], \text{ reg rd} \]

**Description:**
The LDSTUB instruction moves an unsigned byte from memory into the destination register, \( r[rd] \), and rewrites the same byte in memory to all ones, while preventing asynchronous trap interruptions. In a multiprocessor system, two or more processors executing atomic load/store instructions which address the same byte simultaneously are guaranteed to execute them serially, in some order.

The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched byte is right-justified and zero-extended in \( r[rd] \).

If the instruction following an integer load uses the load's \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

If LDSTUB takes a trap, the contents of the memory address remain unchanged.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**
- data_access_exception

**Format:**

<table>
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<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>simm13</td>
<td></td>
<td></td>
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<th>0</th>
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<tbody>
<tr>
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<td>1</td>
<td>rd</td>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>
LDSTUBA Atomic Load/Store Unsigned Byte LDSTUBA in Alternate space (Privileged Instruction)

Operation: 
address space ← asi
r[rd] ← zero extnd[r[rs1] + r[rs2]]
[r[rs1] + r[rs2]] ← FFFFFFFFH

Assembler Syntax: ldstuba [reg_addr] asi, reg_rd

Description: The LDSTUBA instruction moves an unsigned byte from memory into the destination register, r[rd], and rewrites the same byte in memory to all ones, while preventing asynchronous trap interruptions. In a multiprocessor system, two or more processors executing atomic load/store instructions which address the same byte simultaneously are guaranteed to execute them in some serial order. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2]. The fetched byte is right-justified and zero-extended in r[rd].

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem. If LDSTUBA takes a trap, the contents of the memory address remain unchanged.

Traps: illegal_instruction (if i=1)
privileged_instruction (if S=0)
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<th>24</th>
<th>19</th>
<th>18</th>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
LDUB
Load Unsigned Byte

Operation:  
\[ r[rd] \leftarrow \text{zero extnd}[r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \]

Assembler Syntax:  
\text{ldub}[address], reg rd

Description:  
The LDUB instruction moves an unsigned byte from memory into the destination register, r[rd]. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The fetched byte is right-justified and zero-extended in r[rd].

If LDUB takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s r[rd] register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Programming note: When rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:  
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<tr>
<td>1</td>
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<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>31</th>
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<th>0</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
</tr>
</tbody>
</table>
LDUBA Load Unsigned Byte from Alternate space

(Privileged Instruction)

Operation:  
- address space $\leftrightarrow$ asi
- $r[rd] \leftarrow$ zero extnd[$r[rs1] + r[rs2]]$

Assembler Syntax:  
```
lduba [reg addr],asi,reg rd
```

Description:  
The LDUBA instruction moves an unsigned byte from memory into the destination register, $r[rd]$.  The effective memory address is a combination of the address space value given in the $asi$ field and the address derived by summing the contents of $r[rs1]$ and $r[rs2]$.  The fetched byte is right-justified and zero-extended in $r[rd]$.

If LDUBA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s $r[rd]$ register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Traps:  
- illegal_instruction (if i=1)
- privileged_instruction (if S=0)
- data_access_exception

Format:

```
<p>| | | | | | | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<tr>
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<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

MATRA MHS  79
Rev. A (10/09/96)
LDUH - Load Unsigned Halfword

**Operation:**
\[ r[rd] \leftarrow \text{zero extnd}[r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \]

**Assembler Syntax:**
lduh \[ address \], \text{reg rd}

**Description:**
The LDUH instruction moves an unsigned halfword from memory into the destination register, \( r[rd] \). The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The fetched halfword is right-justified and zero-extended in \( r[rd] \).

If LDUH takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load’s \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

**Traps:**
- memory_address_not_aligned
- data_access_exception

**Format:**

```
  31  30  29  25  24  19  18  14  13  12  5  4  0
  1  1  \text{rd}  \text{0 0 0 0 1 0}  \text{rs1}  \text{i=0}  \text{ignored}  \text{rs2}

  31  30  29  25  24  19  18  14  13  12  0
  1  1  \text{rd}  \text{0 0 0 0 1 0}  \text{rs1}  \text{i=1}  \text{simm13}
```
LDUHA

Load Unsigned Halfword from Alternate space

(Privileged Instruction)

Operation:

\[
\begin{align*}
\text{address space} & \leftarrow \text{asi} \\
r[rd] & \leftarrow \text{zero extnd}[r[rs1] + r[rs2]]
\end{align*}
\]

Assembler Syntax:

\[
\text{lduha } [\text{regaddr} \text{ asi}, \text{reg rd}
\]

Description:

The LDUHA instruction moves an unsigned halfword from memory into the destination register, \( r[rd] \). The effective memory address is a combination of the address space value given in the \( \text{asi} \) field and the address derived by summing the contents of \( r[rs1] \) and \( r[rs2] \). The fetched halfword is right-justified and zero-extended in \( r[rd] \).

If LDUHA takes a trap, the contents of the destination register remain unchanged.

If the instruction following an integer load uses the load's \( r[rd] \) register as a source operand, hardware interlocks add one or more delay cycles depending upon the memory subsystem.

Traps:

- illegal_instruction (if \( i=1 \))
- privileged_instruction (if \( S=0 \))
- memory_address_not_aligned
- data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Operation:**

\[ \text{op1} = (n \text{ XOR } v) \text{ CONCAT } r[rs1]<31:1> \]

if \( Y<0> = 0 \)
\[ \text{op2} = 0, \]
else \( \text{op2} = r[rs2] \text{ OR } \text{sign extnd}(\text{simm13}) \)
\[ r[rd] \]
\[ \text{op1} + \text{op2} \]
\[ Y \]
\[ r[rs1]<0> \text{ CONCAT } Y<31:1> \]
\[ n \]
\[ r[rd]<31> \]
\[ z \]
\[ \text{if } [r[rd]]=0 \text{ then 1, else 0} \]
\[ v \]
\[ (\text{op1}<31> \text{ AND } \text{op2}<31> \text{ AND } \text{not } r[rd]<31>) \]
\[ \text{OR } (\text{not } \text{op1}<31> \text{ AND } \text{not } \text{op2}<31> \text{ AND } r[rd]<31>) \]
\[ c \]
\[ (\text{op1}<31> \text{ AND } \text{op2}<31>) \]
\[ \text{OR } (\text{not } r[rd] \text{ AND } (\text{op1}<31> \text{ OR } \text{op2}<31>)) \]

**Assembler Syntax:**

```
mulscc reg\_rs1, reg\_or\_imm, reg\_rd
```

**Description:**

The multiply step instruction can be used to generate the 64-bit product of two signed or unsigned words. MULScc works as follows:

1. The “incoming partial product” in \( r[rs1] \) is shifted right by one bit and the high-order bit is replaced by the sign of the previous partial product \((n \text{ XOR } v)\). This is operand1.

2. If the least significant bit of the multiplier in the Y register equals zero, then operand2 is set to zero. If the LSB of the Y register equals one, then operand2 becomes the multiplicand, which is either the contents of \( r[rs2] \) if the instruction \( i \text{ field } \) is zero, or sign extnd(\text{simm13}) if the \( i \text{ field } \) is one. Operand2 is then added to operand1 and stored in \( r[rd] \) (the outgoing partial product).

3. The multiplier in the Y register is then shifted right by one bit and its high-order bit is replaced by the least significant bit of the incoming partial product in \( r[rs1] \).

4. The PSR’s integer condition codes are updated according to the addition performed in step 2.

**Traps:**

none

**Format:**

| 31 30 29 25 24 19 18 14 13 12 5 4 0 |
|-------------------------------|-----------------|--------------|
| 1 0 rd 1 0 0 1 0 0 rs1 i=0 ignored rs2 |

| 31 30 29 25 24 19 18 14 13 12 0 |
|-------------------------------|-----------------|--------------|
| 1 0 rd 1 0 0 1 0 0 rs1 i=1 simm13 |
**Inclusive-Or**

**Operation:**
\[ r[rd] \gets r[rs1] \text{ OR } (r[rs2] \text{ or sign extnd(simm13)}) \]

**Assembler Syntax:**
\[ \text{or reg}_{rs1}, \text{ reg}_{or \text{ or } \text{imm}}, \text{ reg}_{rd} \]

**Description:**
This instruction does a bitwise logical OR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \).

**Traps:**
none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>12</th>
<th>5</th>
<th>4</th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>i=0</td>
<td>ignored</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ORcc

Inclusive-Or and modify icc

ORcc

Operation:

\[
\begin{align*}
\text{r[rd]} & \leftarrow \text{r[rs1]} \text{ OR } (\text{r[rs2]} \text{ or sign extnd(simm13)}) \\
\text{n} & \leftarrow \text{r[rd]}<31> \\
\text{z} & \leftarrow \text{if } [\text{r[rd]}]=0 \text{ then } 1, \text{ else } 0 \\
\text{v} & \leftarrow 0 \\
\text{c} & \leftarrow 0
\end{align*}
\]

Assembler Syntax:

\text{orcc reg}_{rs1}, \text{reg}_{or imm}, \text{reg}_{rd}

Description:

This instruction does a bitwise logical OR of the contents of register \text{r[rs1]} with either the contents of \text{r[rs2]} (if bit field \text{i}=0) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \text{i}=1). The result is stored in register \text{r[rd]}. ORcc also modifies all the integer condition codes in the manner described above.

Traps:

none

Format:

\[
\begin{array}{cccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 0 & \text{rd} & 0 & 1 & 0 & 0 & 1 & 0 & \text{rs1} & \text{i}=0 & \text{ignored} & \text{rs2} \\
\hline
1 & 0 & \text{rd} & 0 & 1 & 0 & 0 & 1 & 0 & \text{rs1} & \text{i}=1 & \text{simm13} & \text{rs2} \\
\end{array}
\]
**ORN**

**Inclusive-Or Not**

**ORN**

**Operation:**  
\[ r_{rd} \leftarrow r_{rs1} \text{ OR not(operand2)}, \text{ where } \text{operand2} = (r_{rs2} \text{ or sign extnd(simm13)}) \]

**Assembler Syntax:**  
\text{orn } r_{rs1}, \text{ reg_or_imm, reg}_{rd} \]

**Description:**  
This instruction does a bitwise logical OR of the contents of register \( r_{rs1} \) with the one’s complement of either the contents of \( r_{rs2} \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r_{rd} \).

**Traps:**  
none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>18</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>000110</td>
<td>rs1</td>
<td>( i=0 )</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>000110</td>
<td>rs1</td>
<td>( i=1 )</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ORNcc  Inclusive-Or Not and modify icc  ORNcc

Operation:  \( r[rd] \leftarrow r[rs1] \text{ OR not}(\text{operand2}), \) where operand2 = \( r[rs2] \text{ or sign extnd(simm13)} \)

\[ \begin{align*}
  n & \leftarrow r[rd]<31> \\
  z & \leftarrow \text{if } r[rd]=0 \text{ then } 1, \text{ else } 0 \\
  v & \leftarrow 0 \\
  c & \leftarrow 0
\end{align*} \]

Assembler Syntax:  \( \text{orncc reg}_{rs1}, \text{ reg_or_imm, reg}_{rd} \)

Description:  This instruction does a bitwise logical OR of the contents of register \( r[rs1] \) with the one’s complement of either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \). ORNcc also modifies all the integer condition codes in the manner described above.

Traps:  none

Format:

\[
\begin{array}{cccccccc}
\hline
1 & 0 & rd & 010110 & rs1 & i=0 & \text{ignored} & rs2 \\
\hline
1 & 0 & rd & 010110 & rs1 & i=1 & \text{simm13} \\
\end{array}
\]
RDPSR  Read Processor State Register  RDPSR  (Privileged Instruction)

Operation:  \( r[rd] \rightarrow \text{PSR} \)

Assembler Syntax:  \( rd \ %\text{psr}, \ reg_{rd} \)

Description:  RDPSR copies the contents of the PSR into the register specified by the \( rd \) field.

Traps:  privileged-instruction (if S=0)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>ignored</td>
</tr>
</tbody>
</table>
RDTBR Read Trap Base Register
(Privileged Instruction)

Operation: \( r[rd] \leftarrow TBR \)

Assembler Syntax: \( rd \% tbr, reg_{rd} \)

Description: RDTBR copies the contents of the TBR into the register specified by the \( rd \) field.

Traps: privileged_instruction (if S=0)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
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<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td>ignored</td>
</tr>
</tbody>
</table>
RDWIM  Read Window Invalid Mask register
(Privileged Instruction)

Operation:  \( r[rd] \leftarrow \text{WIM} \)

Assembler Syntax:  \( rd\ %\text{wim},\ reg_{rd} \)

Description:  RDWIM copies the contents of the WIM register into the register specified by the \( rd \) field.

Traps:  privileged_instruction (if S=0)

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
RDY Read Y register

**Operation:**  \[ r[rd] \rightarrow Y \]

**Assembler Syntax:**  \[ rd \ %y, reg_{rd} \]

**Description:** RDY copies the contents of the Y register into the register specified by the \( rd \) field.

**Traps:** none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

ignored
RESTORE

Operation:
\[ \text{ncwp} \leftarrow \text{CWP} + 1 \]
\[ \text{result} \leftarrow r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) \]
\[ \text{CWP} \leftarrow \text{ncwp} \]
\[ r[rd] \leftarrow \text{result} \]

RESTORE does not affect condition codes

Assembler Syntax:
\[ \text{restore reg}_{rs1}, \text{reg}_{or_imm}, \text{reg}_{rd} \]

Description:
RESTORE adds one to the Current Window Pointer (modulo the number of implemented windows) and compares this value against the Window Invalid Mask register. If the new window number corresponds to an invalidated window (WIM AND 2^{\text{ncwp}} = 1), a \text{window_underflow} trap is generated. If the new window number is not invalid (i.e., its corresponding WIM bit is reset), then the contents of \( r[rs1] \) is added to either the contents of \( r[rs2] \) (field bit \( i = 1 \)) or to the 13-bit, sign-extended immediate value contained in the instruction (field bit \( i = 0 \)). Because the CWP has not been updated yet, \( r[rs1] \) and \( r[rs2] \) are read from the currently addressed window (the called window).

The new CWP value is written into the PSR, causing the previous window (the caller’s window) to become the active window. The result of the addition is now written into the \( r[rd] \) register of the restored window.

Note that arithmetic operations involving the CWP are always done modulo the number of implemented windows (8 for the CY7C601).

Traps:
\text{window_underflow}

Format:

\begin{array}{|c|c|c|c|c|c|c|c|}
\hline
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 \ 13 & 12 & 5 & 4 & 0 \\
\hline
1 & 0 & \text{rd} & 1 & 1 & 1 & 1 & 0 & 1 & \text{i=0} & \text{ignored} & \text{rs2} \\
\hline
\end{array}

\begin{array}{|c|c|c|c|c|c|c|c|c|}
\hline
31 & 30 & 29 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 0 \\
\hline
1 & 0 & \text{rd} & 1 & 1 & 1 & 1 & 0 & 1 & \text{i=1} & \text{simm13} \\
\hline
\end{array}
RET

Return from Trap

(Privileged Instruction)

Operation:

\[ \text{ncwp} \leftarrow \text{CWP} + 1 \]
\[ \text{ET} \leftarrow 1 \]
\[ \text{PC} \leftarrow \text{nPC} \]
\[ \text{nPC} \leftarrow r[\text{rs1}] + (r[\text{rs2}] \text{ or sign extnd(simm13)]) \]
\[ \text{CWP} \leftarrow \text{ncwp} \]
\[ S \leftarrow pS \]

Assembler:

\text{rett address}

Description:

RET adds one to the Current Window Pointer (modulo the number of implemented windows) and compares this value against the Window Invalid Mask register. If the new window number corresponds to an invalidated window (WIM AND 2^{\text{ncwp}} = 1), a window_underflow trap is generated. If the new window number is not invalid (i.e., its corresponding WIM bit is reset), then RETT causes a delayed control transfer to the address derived by adding the contents of \( r[\text{rs1}] \) to either the contents of \( r[\text{rs2}] \) (field bit \( i = 1 \)) or to the 13-bit, sign-extended immediate value contained in the instruction (field bit \( i = 0 \)).

Before the control transfer takes place, the new CWP value is written into the PSR, causing the previous window (the one in which the trap was taken) to become the active window. In addition, the PSR’s ET bit is set to one (traps enabled) and the previous Supervisor bit (pS) is restored to the S field.

Although in theory RETT is a delayed control transfer instruction, in practice, RETT must always be immediately preceded by a JMP command, creating a delayed control transfer couple (see Section NO TAG). This has the effect of annulling the delay instruction.

If traps were already enabled before encountering the RETT instruction, an illegal_instruction trap is generated. If traps are not enabled (ET=0) when the RETT is encountered, but (1) the processor is not in supervisor mode (S=0), or (2) the window underflow condition described above occurs, or (3) if either of the two low-order bits of the target address are nonzero, then a reset trap occurs. If a reset trap does occur, the \( n \) field of the TBR encodes the trap condition: privileged_instruction, window_underflow, or memory_address_not_aligned.

Programming note: To re-execute the trapping instruction when returning from a trap handler, use the following sequence:

\[
\text{jmpl} \quad \%17, \%0 \quad \text{! old PC} \\
\text{rett} \quad \%18 \quad \text{! old nPC}
\]

Note that the CY7C601 saves the PC in r[17](local 1) and the nPC in r[18](local 2) of the trap window upon entering a trap. To return to the instruction after the trapping instruction (e.g., when the trapping instruction is emulated), use the sequence:

\[
\text{jmpl} \quad \%18, \%0 \quad \text{! old nPC} \\
\text{rett} \quad \%18 + 4 \quad \text{! old nPC} + 4
\]
RETT

Return from Trap (Privileged Instruction)

Traps:
- illegal_instruction
- reset (privileged_instruction)
- reset (memory_address_not_aligned)
- reset (window_underflow)

Format:

```
  | 31 | 30 | 29 | 25 | 24 | 19 | 18 | 14 | 13 | 12 | 5 | 4 | 0 |
---|----|----|----|----|----|----|----|----|----|----|---|---|---|
1  | 0  | ignored | 1 | 1 | 1 | 0 | 0 | 1 | rs1 | i=0 | ignored | rs2 |
---|----|---------|---|---|---|---|---|---|----|----|----|---|---|---|
1  | 0  | ignored | 1 | 1 | 1 | 0 | 0 | 1 | rs1 | i=1 | simm13 |
```
Operation:  
ncwp ← CWP - 1  
result ← r[rs1] + (r[rs2] or sign extnd(simm13))  
CWP ← ncwp  
r[rd] ← result  
SAVE does not affect condition codes

Assembler Syntax:  
save  reg(rs1),  reg_or_imm,  reg(rd)

Description:  
SAVE subtracts one from the Current Window Pointer (modulo the number of implemented windows) and compares this value against the Window Invalid Mask register. If the new window number corresponds to an invalidated window (WIM AND 2^{ncwp} = 1), a window_overflow trap is generated. If the new window number is not invalid (i.e., its corresponding WIM bit is reset), then the contents of r[rs1] is added to either the contents of r[rs2] (field bit $i=1$) or to the 13-bit, sign-extended immediate value contained in the instruction (field bit $i=0$). Because the CWP has not been updated yet, r[rs1] and r[rs2] are read from the currently addressed window (the calling window).

The new CWP value is written into the PSR, causing the active window to become the previous window, and the called window to become the active window. The result of the addition is now written into the [rd] register of the new window.

Note that arithmetic operations involving the CWP are always done modulo the number of implemented windows (8 for the CY7C601).

Traps:  
window_overflow

Format:

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>==0</td>
<td>ignored</td>
<td>rs2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>==1</td>
</tr>
</tbody>
</table>
SETHI

Set High 22 bits of r register

Operation:
\[ r[rd][31:10] \leftarrow \text{imm22} \]
\[ r[rd][9:0] \leftarrow 0 \]

Assembler Syntax:
sethi const22, reg rd
sethi %hi value, reg rd

Description:
SETHI zeros the ten least significant bits of the contents of \([rd]\) and replaces its high-order 22 bits with \(\text{imm22}\). The condition codes are not affected.

Programming note: SETHI \(0, \%0\) is the preferred instruction to use as a NOP, because it will not increase execution time if it follows a load instruction.

Traps:
none

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>22</th>
<th>21</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>imm22</td>
<td></td>
</tr>
</tbody>
</table>
### SLL

**Operation:**

\[ r[r\text{d}] \leftarrow r[r\text{s1}] \text{ SLL by (r[rs2] or shcnt)} \]

**Assembler Syntax:**

\[ \text{sll reg}_{rs1}, \text{ reg}_{or \_imm}, \text{ reg}_{rd} \]

**Description:**

SLL shifts the contents of \( r[rs1] \) left by the number of bits specified by the shift count, filling the vacated positions with zeros. The shifted results are written into \( r[rd] \). No shift occurs if the shift count is zero.

If the i bit field equals zero, the shift count for SLL is the least significant five bits of the contents of \( r[rs2] \). If the i bit field equals one, the shift count for SLL is the 13-bit, sign extended immediate value, simm13. In the instruction format and the operation description above, the least significant five bits of simm13 is called \( \text{shcnt} \).

This instruction does not modify the condition codes.

**Traps:**

none

**Format:**

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ignored</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
</table>
| 1  | 0  | rd | 1  | 0  | 0  | 1 | 0  | 1 | ignored | |  |  | shcnt 
```
### SRA - Shift Right Arithmetic

**Operation:** \( r[rd] \leftarrow r[rs1] \) SRA by \((r[rs2] \text{ or } \text{shcnt})\)

**Assembler Syntax:**
\[
sra\ reg_{rs1},\ reg_{or\_imm},\ reg_{rd}
\]

**Description:**
SRA shifts the contents of \( r[rs1] \) right by the number of bits specified by the shift count, filling the vacated positions with the MSB of \( r[rs1] \). The shifted results are written into \( r[rd] \). No shift occurs if the shift count is zero.

If the \( i \) bit field equals zero, the shift count for SRA is the least significant five bits of the contents of \( r[rs2] \). If the \( i \) bit field equals one, the shift count for SRA is the 13-bit, sign extended immediate value, simm13. In the instruction format and the operation description above, the least significant five bits of simm13 is called \( \text{shcnt} \).

This instruction does not modify the condition codes.

**Programming note:** A “Shift Left Arithmetic by 1 (and calculate overflow)” can be implemented with an ADDcc instruction.

**Traps:**
none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>i=0</td>
<td>ignored</td>
<td></td>
<td></td>
<td>rs2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>i=1</td>
<td>ignored</td>
<td></td>
<td></td>
<td>shcnt</td>
</tr>
</tbody>
</table>
SRL  
Shift Right Logical  

Operation:  
r[rd] ← r[rs1] SRL by (r[rs2] or shcnt)  

Assembler Syntax:  
srl reg, reg_or_imm, reg  

Description:  
SRL shifts the contents of r[rs1] right by the number of bits specified by the shift count, filling the vacated positions with zeros. The shifted results are written into r[rd]. No shift occurs if the shift count is zero.  

If the i bit field equals zero, the shift count for SRL is the least significant five bits of the contents of r[rs2]. If the i bit field equals one, the shift count for SRL is the 13-bit, sign extended immediate value, simm13. In the instruction format and the operation description above, the least significant five bits of simm13 is called shcnt.  

This instruction does not modify the condition codes.  

Traps:  
none  

Format:  

```
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>100110</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>100110</td>
<td>rs1</td>
<td>i=1</td>
<td>ignored</td>
<td>shcnt</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
**ST Operation:**  
[r[rs1] + (r[rs2] or sign extnd(simm13))] → r[rd]

**Assembler Syntax:**  
`st regrd, [address]`

**Description:**  
The ST instruction moves a word from the destination register, r[rd], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If ST takes a trap, the contents of the memory address remain unchanged.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**  
- memory_address_not_aligned
- data_access_exception

**Format:**

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>rd</td>
<td>1</td>
</tr>
<tr>
<td>30</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>29-25</td>
<td>0 0 0 0 0</td>
<td>rs1</td>
</tr>
<tr>
<td>19-18</td>
<td>i=0</td>
<td>ignored</td>
</tr>
<tr>
<td>14-12</td>
<td>i=1</td>
<td>simm13</td>
</tr>
<tr>
<td>5-4</td>
<td>i=0</td>
<td>ignored</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>rs2</td>
</tr>
</tbody>
</table>
## STA

### Store Word into Alternate space

**(Privileged Instruction)**

**Operation:**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>r[rs1]</td>
<td>r[rs2]</td>
<td>r[rd]</td>
<td>asi</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Assembler Syntax:**

sta regrd, [regaddr] asi

**Description:**

The STA instruction moves a word from the destination register, r[rd], into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of r[rs1] and r[rs2].

If STA takes a trap, the contents of the memory address remain unchanged.

**Traps:**

- illegal_instruction (if i=1)
- privileged_instruction (if S=0)
- memory_address_not_aligned
- data_access_exception

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>9</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

---

MATRA MHS
Rev. A (10/09/96)
STB

Operation:
\[ [r[rs1] + (r[rs2] or sign extnd(simm13))] \rightarrow r[rd] \]

Assembler Syntax:
\[ \text{stb \ reg}_rd, [\text{address}] \]

Description:
The STB instruction moves the least significant byte from the destination register, \( r[rd] \), into memory. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If STB takes a trap, the contents of the memory address remain unchanged.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:
data_access_exception

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
<td>ignored</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
</tr>
</tbody>
</table>
STBA

Store Byte into Alternate space

(Privileged Instruction)

**Operation:**

\[ [r[rs1] + r[rs2]] \rightarrow r[rd] \]

**Assembler Syntax:**

stba \( \text{reg}_{rd} \), \( \text{reg}_{addr} \) asi

synonyms: stuba, staba

**Description:**

The STBA instruction moves the least significant byte from the destination register, \( r[rd] \), into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of \( r[rs1] \) and \( r[rs2] \).

If STBA takes a trap, the contents of the memory address remain unchanged.

**Traps:**

illegal_instruction (if \( i=1 \))
privileged_instruction (if \( S=0 \))
data_access_exception

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
<td>asi</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

**Rev. A (10/09/96)**
**STC**

**Store Coprocessor register**

**Operation:**

\[ [r[rs1] + (r[rs2] or sign extnd(simm13))] \rightarrow c[rd] \]

**Assembler Syntax:**

\[ st \ creg, [address] \]

**Description:**

The STC instruction moves a word from a coprocessor register, c[rd], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If STC takes a trap, memory remains unchanged.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**

- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>rd</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
STCSR

**Store Coprocessor State Register**

**STCSR**

**Operation:**

\[ [r[rs1] + (r[rs2] or sign extnd(simm13))] \rightarrow CSR \]

**Assembler Syntax:**

\[ st \ %csr, \ [address] \]

**Description:**

The STCSR instruction moves the contents of the Coprocessor State Register into memory. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If STCSR takes a trap, the contents of the memory address remain unchanged.

*Programming note:* If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**

- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

**Format:**

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<tr>
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<td>1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
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<td>ignored</td>
<td>rs2</td>
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<td>1</td>
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<td>1</td>
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<td>1</td>
<td>i=1</td>
<td>simm13</td>
<td>simm13</td>
<td>simm13</td>
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</table>

**Revision:**

SPARC V7.0

Rev. A (10/09/96)
STD Store Doubleword

Operation:
[r[rs1] + (r[rs2] or sign extnd(simm13))] \(\rightarrow\) r[rd]
[r[rs1] + (r[rs2] or sign extnd(simm13)) + 4] \(\rightarrow\) r[rd + 1]

Assembler Syntax:
std reg, [address]

Description:
The STD instruction moves a doubleword from the destination register pair, r[rd] and r[rd+1], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If a data_access_exception trap takes place during the effective address memory access, memory remains unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:
memory_address_not_aligned
data_access_exception

Format:

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<td>rd</td>
<td>000111</td>
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<td>i=1</td>
<td>simm13</td>
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</table>
STDA Store Doubleword into Alternate space

(Privileged Instruction)

Operation:

address space ← asi

\[ [r[rs1] + (r[rs2] or sign extnd(simm13))] ← r[rd] \]

\[ [r[rs1] + (r[rs2] or sign extnd(simm13)) + 4] ← r[rd + 1] \]

Assembler Syntax:

\[ \text{stda } \text{reg} \text{rd}, [\text{reg} \text{addr}] \text{asi} \]

Description:

The STDA instruction moves a doubleword from the destination register pair, \( r[rd] \) and \( r[rd+1] \), into memory. The effective memory address is a combination of the address space value given in the \( asi \) field and the address derived by summing the contents of \( r[rs1] \) and \( r[rs2] \). The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If a data access exception trap takes place during the effective address memory access, memory remains unchanged.

Traps:

-illegal_instruction (if \( i=1 \))

-privileged_instruction (if \( S=0 \))

-memory_address_not_aligned

-data_access_exception

Format:

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<td>1</td>
<td>1</td>
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<td>i=0</td>
<td>asi</td>
<td>rs2</td>
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</tr>
</tbody>
</table>
STDC Store Doubleword Coprocessor

Operation:

\[
[r_{rs1} + (r_{rs2} \text{ or sign extnd(simm13))}] \leftrightarrow c[rd] \\
[r_{rs1} + (r_{rs2} \text{ or sign extnd(simm13))} + 4] \leftrightarrow c[rd + 1]
\]

Assembler Syntax:

\[
\text{std } creg_{rd}, \text{ [address]}
\]

Description:

The STDC instruction moves a doubleword from the coprocessor register pair, \(c[rd]\) and \(c[rd+1]\), into memory. The effective memory address is derived by summing the contents of \(r_{rs1}\) and either the contents of \(r_{rs2}\) if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cp_disabled trap will be generated. If a data_access_exception trap takes place during the effective address memory access, memory remains unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:

- cp_disabled
- cp_exception
- memory_address_not_aligned
- data_access_exception

Format:

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<td>1</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
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<td>1</td>
<td>rs1</td>
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</tr>
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</table>
STDCQ

Operation:

\[
\begin{align*}
\text{CQ.ADDR} & \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))] \\
\text{CQ.INSTR} & \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13))} + 4]
\end{align*}
\]

Assembler Syntax:

\[
\text{std } \%\text{cq}, [\text{address}]
\]

Description:
The STDCQ instruction moves the front entry of the Coprocessor Queue into memory. The effective memory address is derived by summing the contents of \(r[rs1]\) and either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one. The address portion of the queue entry is written into memory at the effective address and the instruction portion of the entry is written into memory at the effective address + 4.

If the PSR’s EC bit is set to zero or if no coprocessor is present, a cpDisabled trap will be generated. If a data_access_exception trap takes place during the effective address memory access, memory remains unchanged.

Programming note: If \(rs1\) is set to 0 and \(i\) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:

- cp_disabled
- cp_exception
- privileged_instruction (if S=0)
- memory_address_not_aligned
- data_access_exception

Format:

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<p>| | | | | | | | | | | | | | |</p>
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</tbody>
</table>
```

- \(rs1\)
- \(i\)
- \(i=0\)
- \(i=1\)
- \(simm13\)
Operation:

\[ [r\{rs1\} + (r\{rs2\} or sign extnd(simm13))] \leftarrow f\{rd\} \]
\[ [r\{rs1\} + (r\{rs2\} or sign extnd(simm13)) + 4] \leftarrow f\{rd + 1\} \]

Assembler Syntax:

\texttt{std reg0, [address]}

Description:

The STDF instruction moves a doubleword from the floating-point register pair, \( f\{rd\} \) and \( f\{rd+1\} \), into memory. The effective memory address is derived by summing the contents of \( r\{rs1\} \) and either the contents of \( r\{rs2\} \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one. The most significant word in the even-numbered destination register is written into memory at the effective address and the least significant memory word in the next odd-numbered register is written into memory at the effective address + 4.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If a trap takes place, memory remains unchanged.

\textit{Programming note:} If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:

- \texttt{fp_disabled}
- \texttt{fp_exception*}
- \texttt{memory_address_notAligned}
- \texttt{data_access_exception}

Format:

\[
\begin{array}{ccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & rd & 100111 & rs1 & i=0 & ignored & rs2 \\
\end{array}
\]

\[
\begin{array}{ccccccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 19 & 18 & 14 & 13 & 12 & 0 \\
1 & 1 & rd & 100111 & rs1 & i=1 & simm13 \\
\end{array}
\]

* NOTE: An attempt to execute \textit{any} FP instruction will cause a pending FP exception to be recognized by the integer unit.
**STDFQ**

*Store Doubleword Floating-Point Queue (Privileged Instruction)*

**Operation:**

\[
\begin{align*}
[r[rs1] + (r[rs2] \text{ or sign extnd(simm13)])] & \rightarrow \text{FQ.ADDR} \\
[r[rs1] + (r[rs2] \text{ or sign extnd(simm13)}) + 4] & \rightarrow \text{FQ.INSTR}
\end{align*}
\]

**Assembler Syntax:**

```
std %fq, [address]
```

**Description:**

The STDFQ instruction moves the front entry of the floating-point queue into memory. The effective memory address is derived by summing the contents of \(r[rs1]\) and either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one. The address portion of the queue entry is written into memory at the effective address and the instruction portion of the entry is written into memory at the effective address + 4.

If the FPU is in exception mode, the queue is then advanced to the next entry, or it becomes empty (as indicated by the \(qne\) bit in the FSR).

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If a trap takes place, memory remains unchanged.

*Programming note:* If \(rs1\) is set to 0 and \(i\) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**

- fp_disabled
- fp_exception*
- privileged_instruction (if \(S=0\))
- memory_address_not_aligned
- data_access_exception

**Format:**

```
0 4 12 13 14 18 19 24 25 29 30 31
|   1 |  1 |  rd | 1 0 0 1 1 0 | rs1 | =0 | ignored | rs2 |
```

```
0 4 12 13 14 18 19 24 25 29 30 31
|   1 |  1 |  rd | 1 0 0 1 1 0 | rs1 | =1 | simm13 |
```

*NOTE:* An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
**STF**

**Operation:** 
\[ r[rs1] + (r[rs2] \text{ or } \text{sign extnd(simm13)}) \leftarrow f[rd] \]

**Assembler Syntax:**
\[ st \ freg_{rd}, [address] \]

**Description:**
The STF instruction moves a word from a floating-point register, f[rd], into memory. The effective memory address is derived by summing the contents of f[rs1] and either the contents of f[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an fp_disabled trap will be generated. If STF takes a trap, memory remains unchanged.

*Programming note:* If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

**Traps:**
- fp_disabled
- fp_exception*
- memory_address_not_aligned
- data_access_exception

**Format:**

```
  31 30 29 25 24 19 18 14 13 12  5  4  0
  1 1  rd 1 0 0 1 0 0  rs1  i=0  ignored  rs2

  31 30 29 25 24 19 18 14 13 12  0
  1 1  rd 1 0 0 1 0 0  rs1  i=1  simm13
```

* NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
STFSR

Store Floating-Point State Register

Operation: \([r[rs1] + (r[rs2] \text{ or sign extnd(simm13))}] \rightarrow \text{FSR}\)

Assembler Syntax: \(\text{st } \%\text{fsr}, [\text{address}]\)

Description: The STFSR instruction moves the contents of the Floating-Point State Register into memory. The effective memory address is derived by summing the contents of \(r[rs1]\) and either the contents of \(r[rs2]\) if the instruction’s \(i\) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \(i\) equals one. This instruction will wait for all pending FPops to complete execution before it writes the FSR into memory.

If the PSR’s EF bit is set to zero or if no floating-point unit is present, an \(\text{fp\_disabled}\) trap will be generated. If STFSR takes a trap, the contents of the memory address remain unchanged.

Programming note: If \(rs1\) is set to 0 and \(i\) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps: \(\text{fp\_disabled}\)  
\(\text{fp\_exception}^*\)  
\(\text{memory\_address\_not\_aligned}\)  
\(\text{data\_access\_exception}\)

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\(^*\) NOTE: An attempt to execute any FP instruction will cause a pending FP exception to be recognized by the integer unit.
STH

Store Halfword

Operation: \([\text{r}[\text{rs1}]] + (\text{r}[\text{rs2} \text{ or sign extnd(simm13) }]) \rightarrow \text{r}[\text{rd}]\)

Assembler Syntax: `sth rd \_ [address]` synonyms: stuh, stsh

Description:
The STH instruction moves the least significant halfword from the destination register, r[rd], into memory. The effective memory address is derived by summing the contents of r[rs1] and either the contents of r[rs2] if the instruction’s i bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if i equals one.

If STH takes a trap, the contents of the memory address remain unchanged.

Programming note: If rs1 is set to 0 and i is set to 1, any location in the lowest or highest 4 kbytes of an address space can be written to without setting up a register.

Traps:
- memory_address_not_aligned
- data_access_exception

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<td>rs1</td>
<td>i=0</td>
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<td>i=1</td>
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</table>
STHA Store Halfword into Alternate space

(Privileged Instruction)

**Operation:**
address space ← asi

\([r[rs1] + r[rs2] \text{ or sign extnd(simm13)]}] ← r[rd]\)

**Assembler Syntax:**

```
stha reg rd, [address]
synonyms: stuh, stsha
```

**Description:**
The STHA instruction moves the least significant halfword from the destination register, \(r[rd]\), into memory. The effective memory address is a combination of the address space value given in the asi field and the address derived by summing the contents of \(r[rs1]\) and \(r[rs2]\).

If STHA takes a trap, the contents of the memory address remain unchanged.

**Traps:**
- illegal_instruction (if \(i=1\))
- privileged_instruction (if \(S=0\))
- memory_address_not_aligned
- data_access_exception

**Format:**

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 1  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| rd | 0 | 1 | 0 | 1 | 1 | 0 | rs1 | i=0 | asi |    | rs2 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
```
SUB

**Operation:**
\[ r[rd] \leftarrow r[rs1] \cdot (r[rs2] \text{ or sign extnd(simmm13)}) \]

**Assembler Syntax:**
```
sub reg_rs1, reg_or_imm, reg_rd
```

**Description:**
The `SUB` instruction subtracts either the contents of the register named in the `rs2` field, \( r[rs2] \), if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one, from register \( r[rs1] \). The result is placed in the register specified in the \( rd \) field.

**Traps:**
none

**Format:**

```
  | 31 | 30 | 29 | 25 | 24 | 19 | 18 | 14 | 13 | 12 | 5 | 4 | 0
---|----|----|----|----|----|----|----|----|----|----|---|---|---
1  | 0  | rd | 0 0 0 1 0 0 | rs1 | i=0 | ignored |  |  |  |  |  |  |  |
3  | 1  | 0  | rd | 0 0 0 1 0 0 | rs1 | i=1 | simm13 |  |  |  |  |  |  |
```
**SUBcc**  
*Subtract and modify icc*

**Operation:**  
r[rd] ← r[rs1] - operand2, where operand2 = (r[rs2] or sign extnd(simm13))  
n ← r[rd]<31>  
z ← if r[rd] =0 then 1, else 0  
v ← (r[rs1]<31> AND not operand2<31> AND not r[rd]<31>)  
2 OR (not r[rs1]<31> AND operand2<31> AND r[rd]<31>)  
c ← (not r[rs1]<31> AND operand2<31>)  
3 OR (r[rd]<31> AND (not r[rs1]<31> OR operand2<31>))

**Assembler Syntax:**  
`subcc regrs1, reg_or_imm, regrd`

**Description:**  
The SUBcc instruction subtracts either the contents of register r[rs2] (if the instruction’s `i` bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if `i` equals one) from register r[rs1]. The result is placed in register r[rd]. In addition, SUBcc modifies all the integer condition codes in the manner described above.

*Programming note:* A SUBcc instruction with `rd` = 0 can be used for signed and unsigned integer comparison.

**Traps:**

none

**Format:**

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
</tr>
</tbody>
</table>
```

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
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<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=1</td>
</tr>
</tbody>
</table>
```
SUBX

Subtract with Carry

Operation:
\[ r[rd] \leftarrow r[rs1] - (r[rs2] \text{ or sign extnd(simm13)}) - c \]

Assembler Syntax:
\[
\text{subx } \text{reg_rs1, reg_or_imm, reg_rd}
\]

Description:
SUBX subtracts either the contents of register \( r[rs2] \) (if the instruction’s \( i \) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \( i \) equals one) from register \( r[rs1] \). It then subtracts the PSR’s carry bit \( (c) \) from that result. The final result is placed in the register specified in the \( rd \) field.

Traps:
none

Format:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>001100</td>
<td>rs1</td>
<td>( i=0 )</td>
<td>ignored</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>001100</td>
<td>rs1</td>
<td>( i=1 )</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
**SUBXcc**  Subtract with Carry and modify icc

**Operation:**

\[ r[rd] \leftarrow r[rs1] - \text{operand2} - c, \text{ where } \text{operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]

- **n** \( \leftarrow r[rd]<31> \)
- **z** \( \leftarrow \text{if } r[rd] = 0 \text{ then } 1, \text{ else } 0 \)
- **v** \( \leftarrow (r[rs1]<31> \text{ AND not operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND operand2}<31> \text{ AND } r[rd]<31>) \)
- **c** \( \leftarrow (\text{not } r[rs1]<31> \text{ AND operand2}<31>) \text{ OR (r[rd]<31> AND (not } r[rs1]<31> \text{ OR operand2}<31>)) \)

**Assembler Syntax:**

\text{subxcc reg,_, or_imm, reg}

**Description:**

SUBXcc subtracts either the contents of register \( r[rs2] \) (if the instruction’s \( i \) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \( i \) equals one) from register \( r[rs1] \). It then subtracts the PSR’s carry bit \( (c) \) from that result. The final result is placed in the register specified in the \( rd \) field. In addition, SUBXcc modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

```
  31  30  29  25  24  19  18  14  13  12  5  4  0
  1  0  rd  0 1 1 1 0 0  rs1 i=0 ignored rs2
  31  30  29  25  24  19  18  14  13  12  0
  1  0  rd  0 1 1 1 0 0  rs1 i=1 simm13
```
SWAP

Swap r register with memory

Operation:
\[ \text{word} \leftarrow [r[rs1] + (r[rs2] \text{ or sign extnd(simm13)])] \]
\[ \text{temp} \leftarrow [r[rd]] \]
\[ r[rd] \leftarrow \text{word} \]
\[ r[rs1] + (r[rs2] \text{ or sign extnd(simm13)]) \leftarrow \text{temp} \]

Assembler Syntax:
\[ \text{swap } [\text{source}], \text{reg}_{rd} \]

Description:
SWAP atomically exchanges the contents of \( r[rd] \) with the contents of a memory location, i.e., without allowing asynchronous trap interruptions. In a multiprocessor system, two or more processors executing SWAP instructions simultaneously are guaranteed to execute them serially, in some order. The effective memory address is derived by summing the contents of \( r[rs1] \) and either the contents of \( r[rs2] \) if the instruction’s \( i \) bit equals zero, or the 13-bit, sign-extended immediate operand contained in the instruction if \( i \) equals one.

If SWAP takes a trap, the contents of the memory address and the destination register remain unchanged.

Programming note: If \( rs1 \) is set to 0 and \( i \) is set to 1, any location in the lowest or highest 4 kbytes of an address space can be accessed without setting up a register.

Traps:
- memory_address_not_aligned
- data_access_exception

Format:

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & \text{rd} & 001111 & \text{rs1} & i=0 & \text{ignored} & \text{rs2} \\
\end{array}
\]

\[
\begin{array}{cccccccc}
31 & 30 & 29 & 28 & 27 & 26 & 25 & 24 & 19 & 18 & 14 & 13 & 12 & 5 & 4 & 0 \\
1 & 1 & \text{rd} & 001111 & \text{rs1} & i=1 & \text{simm13} \\
\end{array}
\]
SWAPA  
Swap \textit{r register} with memory in Alternate space  

(Privileged Instruction)

\textbf{Operation:} 
address space $\leftrightarrow$ asi  
word $\leftrightarrow$ \texttt{[r[rs1] + r[rs2]]}  
temp $\leftrightarrow$ \texttt{r[rd]}  
\texttt{r[rd]} $\leftrightarrow$ word  
\texttt{[r[rs1] + r[rs2]]} $\leftrightarrow$ temp

\textbf{Assembler Syntax:} 
\texttt{swapa [regsource] asi, reg rd}

\textbf{Description:} SWAPA atomically exchanges the contents of \texttt{r[rd]} with the contents of a memory location, i.e., without allowing asynchronous trap interruptions. In a multiprocessor system, two or more processors executing SWAPA instructions simultaneously are guaranteed to execute them serially, in some order.

The effective memory address is a combination of the address space value given in the \texttt{asi} field and the address derived by summing the contents of \texttt{r[rs1]} and \texttt{r[rs2]}.

If SWAPA takes a trap, the contents of the memory address and the destination register remain unchanged.

\textbf{Traps:} 
illegal\_instruction (if \texttt{i=1})  
privileged\_instruction (if \texttt{S=0})  
memory\_address\_not\_aligned  
data\_access\_exception

\textbf{Format:}

\begin{center}
\begin{tabular}{cccccccc}
\hline
1 & 1 & \texttt{rd} & 0 & 1 & 1 & 1 & 1 & \texttt{rs1} & \texttt{i=0} & \texttt{asi} & \texttt{rs2}
\end{tabular}
\end{center}
TADDcc: Tagged Add and modify ICC

Operation:
\[ r[rd] \leftarrow r[rs1] + \text{operand2}, \text{where operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]
\[ n \leftarrow r[rd]<31> \]
\[ z \leftarrow \text{if } r[rd]=0 \text{ then } 1, \text{ else } 0 \]
\[ v \leftarrow (r[rs1]<31> \text{ AND operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR (not } r[rs1]<31> \text{ AND not operand2}<31> \text{ AND } r[rd]<31>) \text{ OR (} r[rs1]<1:0> \neq 0 \text{ OR operand2}<1:0> \neq 0 \text{)} \]
\[ c \leftarrow (r[rs1]<31> \text{ AND operand2}<31> \text{ OR (not } r[rd]<31> \text{ AND (} r[rs1]<31> \text{ OR operand2}<31>\)) \]

Assembler Syntax:
taddcc reg, reg_or_imm, reg

Description:
TADDcc adds the contents of r[rs1] to either the contents of r[rs2] if the instruction’s i bit equals zero, or to a 13-bit, sign-extended immediate operand if i equals one. The result is placed in the register specified in the rd field. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero. TADDcc modifies all the integer condition codes in the manner described above.

Traps:
none

Format:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
</tr>
</tbody>
</table>
TADDccTV  Tagged Add (modify icc) Trap on Overflow TADDccTV

Operation:  
result ← r[rs1] + operand2, where operand 2 = (r[rs2] or sign extnd(simm13))

$tv ← (r[rs1]<31> AND operand2<31> AND not r[rd]<31>)$
$OR (not r[rs1]<31> AND not operand2<31> AND r[rd]<31>)$
$OR (r[rs1]<1:0> ≠ 0 OR operand2<1:0> ≠ 0)$

if $tv = 1$, then tag overflow trap; else

$n ← r[rd]<31>$
$z ← if r[rd]=0 then 1, else 0$
$v ← tv$
$c ← (r[rs1]<31> AND operand2<31>)$
$OR (not r[rd]<31> AND (r[rs1]<31> OR operand2<31>))$

$r[rd] ← result$

Assembler Syntax:  
tagdctv reg,reg_or_imm,reg

Description:  
TADDccTV adds the contents of r[rs1] to either the contents of r[rs2] if the instruction’s i bit equals zero, or to a 13-bit, sign-extended immediate operand if i equals one. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero.

If TADDccTV detects an overflow condition, a tag_overflow trap is generated and the destination register and condition codes remain unchanged. If no overflow is detected, TADDccTV places the result in the register specified in the rd field and modifies all the integer condition codes in the manner described above (the overflow bit is, of course, set to zero).

Traps:  
tag_overflow

Format:  

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 1  | 0  | 0 | 0 | 1 | 0 | rs1 | =0 | ignored | rs2 | 0 |
| 1  | 0  | rd | 1  | 0  | 0 | 0 | 1 | 0 | rs1 | =1 | simm13 | 0 |
Ticc

Trap on integer condition codes

Operation: If condition true, then trap_instruction;

\[
tt \leftarrow 128 + [r[rs1] + (r[rs2] or sign extnd(simm13))] <6:0>
\]

else PC \leftarrow nPC

nPC \leftarrow nPC + 4

Assembler

Syntax:

\[
\text{ta[,a]} \quad \text{label}
\]

\[
\text{tn[,a]} \quad \text{label}
\]

\[
\text{tne[,a]} \quad \text{label} \quad \text{synonym: tnz}
\]

\[
\text{tc[,a]} \quad \text{label} \quad \text{synonym: tz}
\]

\[
\text{tg[,a]} \quad \text{label}
\]

\[
\text{tle[,a]} \quad \text{label}
\]

\[
\text{tlu[,a]} \quad \text{label}
\]

\[
\text{tcc[,a]} \quad \text{label} \quad \text{synonym: tgeu}
\]

\[
\text{tcs[,a]} \quad \text{label} \quad \text{synonym: tlu}
\]

\[
\text{tpos[,a]} \quad \text{label}
\]

\[
\text{tneg[,a]} \quad \text{label}
\]

\[
\text{tvc[,a]} \quad \text{label}
\]

\[
\text{tvs[,a]} \quad \text{label}
\]

Description: A Ticc instruction evaluates specific integer condition code combinations (from the PSR’s icc field) based on the trap type as specified by the value in the instruction’s cond field. If the specified combination of condition codes evaluates as true, and there are no higher-priority traps pending, then a trap_instruction trap is generated. If the condition codes evaluate as false, the trap is not generated.

If a trap_instruction trap is generated, the tt field of the Trap Base Register (TBR) is written with 128 plus the least significant seven bits of r[rs1] plus either r[rs2] (bit field \( i = 0 \)) or the 13-bit sign-extended immediate value contained in the instruction (bit field \( i = 1 \)). See Section NO TAG for the complete definition of a trap.

Traps: trap_instruction
### Ticc

**Trap on integer condition codes**

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Cond.</th>
<th>Operation</th>
<th>ice Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>TN</td>
<td>0000</td>
<td>Trap Never</td>
<td>No test</td>
</tr>
<tr>
<td>TE</td>
<td>0001</td>
<td>Trap on Equal</td>
<td>z</td>
</tr>
<tr>
<td>TLE</td>
<td>0010</td>
<td>Trap on Less or Equal</td>
<td>z OR (n XOR v)</td>
</tr>
<tr>
<td>TL</td>
<td>0011</td>
<td>Trap on Less</td>
<td>n XOR v</td>
</tr>
<tr>
<td>TLEU</td>
<td>0100</td>
<td>Trap on Less or Equal, Unsigned</td>
<td>c OR z</td>
</tr>
<tr>
<td>TCS</td>
<td>0101</td>
<td>Trap on Carry Set (Less than, Unsigned)</td>
<td>c</td>
</tr>
<tr>
<td>TNEG</td>
<td>0110</td>
<td>Trap on Negative</td>
<td>n</td>
</tr>
<tr>
<td>TVS</td>
<td>0111</td>
<td>Trap on Overflow Set</td>
<td>v</td>
</tr>
<tr>
<td>TA</td>
<td>1000</td>
<td>Trap Always</td>
<td>No test</td>
</tr>
<tr>
<td>TNE</td>
<td>1001</td>
<td>Trap on Not Equal</td>
<td>not z</td>
</tr>
<tr>
<td>TG</td>
<td>1010</td>
<td>Trap on Greater</td>
<td>not(z OR (n XOR v))</td>
</tr>
<tr>
<td>TGE</td>
<td>1011</td>
<td>Trap on Greater or Equal</td>
<td>not(n XOR v)</td>
</tr>
<tr>
<td>TGU</td>
<td>1100</td>
<td>Trap on Greater, Unsigned</td>
<td>not(c OR z)</td>
</tr>
<tr>
<td>TCC</td>
<td>1101</td>
<td>Trap on Carry Clear (Greater than or Equal, Unsigned)</td>
<td>not c</td>
</tr>
<tr>
<td>TPOS</td>
<td>1110</td>
<td>Trap on Positive</td>
<td>not n</td>
</tr>
<tr>
<td>TVC</td>
<td>1111</td>
<td>Trap on Overflow Clear</td>
<td>not v</td>
</tr>
</tbody>
</table>

#### Format:

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<table>
<thead>
<tr>
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<th>30</th>
<th>29</th>
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<th>12</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ign.</td>
<td>cond.</td>
<td>1 1 1 0 1 0</td>
<td>rs1</td>
<td>/=0</td>
<td>ignored</td>
<td></td>
<td>rs2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

```
<table>
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<tr>
<th>31</th>
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<th>28</th>
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<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>ign.</td>
<td>cond.</td>
<td>1 1 1 0 1 0</td>
<td>rs1</td>
<td>/=1</td>
<td>simm13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

ign. = ignored  
cond. = condition
**TSUBcc**

**Tagged Subtract and modify icc**

**TSUBcc**

**Operation:** 
\[ r[rd] \leftarrow r[rs1] - \text{operand2}, \text{where operand2} = (r[rs2] \text{ or sign extnd(simm13)}) \]

\[ n \leftarrow r[rd]<31> \]

\[ z \leftarrow \text{if } r[rd]=0 \text{ then 1, else 0} \]

\[ v \leftarrow (r[rs1]<31> \text{ AND not operand2}<31> \text{ AND not } r[rd]<31>) \text{ OR } (\text{not } r[rs1]<31> \text{ AND operand2}<31> \text{ AND } r[rd]<31>) \text{ OR } (r[rs1]<1:0> \neq 0 \text{ OR operand2}<1:0> \neq 0) \]

\[ c \leftarrow (\text{not } r[rs1]<31> \text{ AND operand2}<31> \text{ OR } (r[rd]<31> \text{ AND } (\text{not } r[rs1]<31> \text{ OR operand2}<31>)) \]

**Assembler Syntax:**

\[ \text{tsubcc } \text{reg}_{rs1}, \text{ reg}_{or}_{imm}, \text{ reg}_{rd} \]

**Description:**

TSUBcc subtracts either the contents of register \( r[rs2] \) (if the instruction’s \( i \) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \( i \) equals one) from register \( r[rs1] \). The result is placed in the register specified in the \( rd \) field. In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero. TSUBcc modifies all the integer condition codes in the manner described above.

**Traps:**

none

**Format:**

```plaintext
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
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<th>12</th>
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<th>4</th>
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<tbody>
<tr>
<td>1</td>
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<td>rd</td>
<td>1</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>i=0</td>
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<td>rs2</td>
<td></td>
</tr>
</tbody>
</table>
```

```plaintext
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
<th>19</th>
<th>18</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>i=1</td>
<td>simm13</td>
</tr>
</tbody>
</table>
```
Operation:

\[ \text{result} \leftarrow \text{rs1} - \text{operand2}, \text{where operand2} = (\text{rs2} \text{ or sign extnd(simm13)}) \]

\[ tv \leftarrow (\text{rs1}<31> \text{ AND not operand2}<31> \text{ AND not rd}<31>) \text{ OR (not rs1}<31> \text{ AND operand2}<31> \text{ AND rd}<31>) \]

\[ \text{tv} \leftarrow (\text{rs1}<31> \text{ AND not operand2}<31> \text{ AND not rd}<31>) \text{ OR (not rs1}<31> \text{ AND operand2}<31> \text{ AND rd}<31>) \]

if \( tv = 1 \), then tag overflow trap; else

\[ n \leftarrow \text{rd}<31> \]

\[ z \leftarrow \text{if rd}<31>\text{ then 1, else 0} \]

\[ v \leftarrow tv \]

\[ c \leftarrow (\text{not(rs1}<31>) \text{ AND operand2}<31> \text{ OR (rd}<31> \text{ AND (not(rs1}<31>) \text{ OR operand2}<31>))) \]

\[ \text{rd} \leftarrow \text{result} \]

Assembler Syntax:

\text{tsubccvt reg}_{rs1}, \text{reg}_{or_{imm}}, \text{reg}_{rd} \]

Description:

TSUBccTV subtracts either the contents of register \( \text{rs2} \) (if the instruction’s \( i \) bit equals zero) or the 13-bit, sign-extended immediate operand contained in the instruction (if \( i \) equals one) from register \( \text{rs1} \). In addition to the normal arithmetic overflow, an overflow condition also exists if bit 1 or bit 0 of either operand is not zero.

If TSUBccTV detects an overflow condition, a tag overflow trap is generated and the destination register and condition codes remain unchanged. If no overflow is detected, TSUBccTV places the result in the register specified in the \( rd \) field and modifies all the integer condition codes in the manner described above (the overflow bit is, of course, set to zero).

Traps:

tag\_overflow

Format:

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 1  | 0  | rd | 10  | 00  | 11 | rs1 | == | 0   | ignored |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| 1  | 0  | rd | 10  | 00  | 11 | rs1 | == | 1   | simm13 |
```
### UNIMP

**Operation:** illegal instruction trap

**Assembler Syntax:** unimp const22

**Description:** Executing the UNIMP instruction causes an immediate illegal_instruction trap. The value in the const22 field is ignored.

*Programming note:* UNIMP can be used as part of the protocol for calling a function that is expected to return an aggregate value, such as a C-language structure.

1. An UNIMP instruction is placed after (not in) the delay slot after the CALL instruction in the calling function.
2. If the called function is expecting to return a structure, it will find the size of the structure that the caller expects to be returned as the const22 operand of the UNIMP instruction. The called function can check the opcode to make sure it is indeed UNIMP.
3. If the function is not going to return a structure, upon returning, it attempts to execute UNIMP rather than skipping over it as it should. This causes the program to terminate. The behavior adds some run-time checking to an interface that cannot be checked properly at compile time.

**Traps:** illegal_instruction

**Format:**

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<table>
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<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
<th>24</th>
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<th>0</th>
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</thead>
<tbody>
<tr>
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<td>0</td>
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<td>0</td>
<td>const22</td>
<td></td>
</tr>
</tbody>
</table>
```
WRPSR does a bitwise logical XOR of the contents of register r[rs1] with either the contents of r[rs2] (if bit field i=0) or the 13-bit sign-extended immediate value contained in the instruction (if bit field i=1). The result is written into the writable subfields of the PSR. However, if the result’s CWP field would point to an unimplemented window, an illegal_instruction trap is generated and the PSR remains unchanged.

WRPSR is a delayed-write instruction:

1. If any of the three instructions following a WRPSR uses any PSR field that WRPSR modified, the value of that field is unpredictable. Note that any instruction which references a non-global register makes use of the CWP, so following WRPSR with three NOPs would be the safest course.

2. If a WRPSR instruction is updating the PSR’s Processor Interrupt Level (PIL) to a new value and is simultaneously setting Enable Traps (ET) to one, this could result in an interrupt trap at a level equal to the old PIL value.

3. If any of the three instructions after a WRPSR instruction reads the modified PSR, the value read is unpredictable.

4. If any of the three instructions after a WRPSR is trapped, a subsequent RDPSR in the trap handler will get the register’s new value.

Programming note: Two WRPSR instructions should be used when enabling traps and changing the PIL value. The first WRPSR should specify ET=0 with the new PIL value, and the second should specify ET=1 with the new PIL value.

Traps: illegal_instruction
privileged_instruction (if S=0)

Format:

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<td>0</td>
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<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td></td>
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<tbody>
<tr>
<td>1</td>
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<td>0</td>
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<td>1</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
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</tr>
</tbody>
</table>
WRTBR
Write Trap Base Register
(Privileged Instruction)

Operation: TBR ← r[rs1] XOR (r[rs2] or sign extnd(simm13))

Assembler Syntax: wr reg, reg_or_imm, %tbr

Description: WRTBR does a bitwise logical XOR of the contents of register r[rs1] with either the contents of r[rs2] (if bit field i=0) or the 13-bit sign-extended immediate value contained in the instruction (if bit field i=1). The result is written into the Trap Base Address field of the TBR.

WRTBR is a delayed-write instruction:
1. If any of the three instructions following a WRTBR causes a trap, the TBA used may be either the old or the new value.
2. If any of the three instructions after a WRTBR is trapped, a subsequent RDTBR in the trap handler will get the register’s new TBA value.

Traps: privileged_instruction (if S=0)

Format:

```
31 30 29 25 24 19 18 14 13 12  5 4  0
1 0 ignored 1 1 0  0  1  1  rs1 i=0 ignored    rs2
```

```
31 30 29 25 24 19 18 14 13 12  0
1 0 ignored 1 1 0  0  1  1  rs1 i=1 simm13
```
**WRWIM**

**Write Window Invalid Mask register**

*(Privileged Instruction)*

**Operation:**

WIM ← r[rs1] XOR (r[rs2] or sign extnd(simm13))

**Assembler Syntax:**

`wr reg_rs1, reg_or_imm, %wim`

**Description:**

WRWIM does a bitwise logical XOR of the contents of register r[rs1] with either the contents of r[rs2] (if bit field i=0) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field i=1). The result is written into the writable bits of the WIM register.

WRWIM is a delayed-write instruction:

1. If any of the three instructions following a WRWIM is a SAVE, RESTORE, or RETT, the occurrence of window overflow and window underflow is unpredictable.
2. If any of the three instructions after a WRWIM instruction reads the modified WIM, the value read is unpredictable.
3. If any of the three instructions after a WRWIM is trapped, a subsequent RDWIM in the trap handler will get the register’s new value.

**Traps:**

privileged_instruction (if S=0)

**Format:**

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<tbody>
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<td>ignored</td>
<td>1 1 0 0 1 0</td>
<td>rs1</td>
<td>i=0</td>
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<td>rs2</td>
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<tbody>
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<td>1 0</td>
<td>ignored</td>
<td>1 1 0 0 1 0</td>
<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
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</tr>
</tbody>
</table>
WRY

Write Y register

Operation:

\[ Y \leftarrow r[rs1] \text{ XOR } (r[rs2] \text{ or sign extnd(simm13)}) \]

Assembler Syntax:

\[ \text{wr reg}_{rs1}, \text{ reg}_{or\_imm}, \%y \]

Description:

WRY does a bitwise logical XOR of the contents of register \( r[rs1] \) with either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is written into the Y register.

WRY is a delayed-write instruction:

1. If any of the three instructions following a WRY is a MULSc or a RDY, the value of Y used is unpredictable.
2. If any of the three instructions after a WRY instruction reads the modified Y register, the value read is unpredictable.
3. If any of the three instructions after a WRY is trapped, a subsequent RDY in the trap handler will get the register’s new value.

Traps:

none

Format:

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<th>25</th>
<th>24</th>
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<th>4</th>
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</tr>
</thead>
<tbody>
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<td>ignored</td>
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<td>1</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>rs1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
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<table>
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<th>29</th>
<th>25</th>
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<td>ignored</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>rs1</td>
<td>i=1</td>
</tr>
</tbody>
</table>
XNOR  Exclusive-Nor  XNOR

Operation:  \[ r[rd] \leftarrow r[rs1] \text{ XOR not}(r[rs2] \text{ or sign extnd(simm13)}) \]

Assembler Syntax:  xnor  reg.rs1,  reg.or_imm,  reg.rd

Description:  This instruction does a bitwise logical XOR of the contents of register r[rs1] with the one’s complement of either the contents of r[rs2] (if bit field i=0) or the 13-bit sign-extended immediate value contained in the instruction (if bit field i=1). The result is stored in register r[rd].

Traps:  none

Format:

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<tr>
<th>31</th>
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<th>29</th>
<th>25</th>
<th>24</th>
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<th>4</th>
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<td>rd</td>
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<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td>i=0</td>
<td>ignored</td>
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<th>30</th>
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<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>rd</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td>simm13</td>
</tr>
</tbody>
</table>
**XNORcc**  Exclusive-Nor and modify icc  **XNORcc**

**Operation:**
\[ r[rd] \leftarrow r[rs1] \text{ XOR } \overline{r[rs2]} \text{ or sign extnd}(\text{simm13}) \]

- \( n \leftarrow r[rd] < 31 > \)
- \( z \leftarrow \text{if } r[rd] = 0 \text{ then 1, else 0} \)
- \( v \leftarrow 0 \)
- \( c \leftarrow 0 \)

**Assembler Syntax:**
\[ \text{xnorcc reg}_{rs1}, \text{ reg}_or_{imm}, \text{ reg}_{rd} \]

**Description:**
This instruction does a bitwise logical XOR of the contents of register \( r[rs1] \) with the one’s complement of either the contents of \( r[rs2] \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r[rd] \). XNORcc also modifies all the integer condition codes in the manner described above.

**Traps:**
none

**Format:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>25</th>
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<th>4</th>
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<td>rd</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>i=0</td>
<td>ignored</td>
<td>rs2</td>
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<td>1</td>
<td>1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
<td></td>
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</tbody>
</table>
XOR

Exclusive-Or

Operation:
\[ r[rd] \leftarrow r[rs1] \text{ XOR } (r[rs2] \text{ or sign extnd(simm13))} \]

Assembler Syntax:
\[ \text{xor } reg_{rs1}, \text{ reg_or_imm, reg}_{rd} \]

Description:
This instruction does a bitwise logical XOR of the contents of register \(r[rs1]\) with either the contents of \(r[rs2]\) (if bit field \(i=0\)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \(i=1\)). The result is stored in register \(r[rd]\).

Traps:
none

Format:

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<th>25</th>
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<tbody>
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<td>0</td>
<td>rd</td>
<td>0 0 0 0 1 1</td>
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<td>rd</td>
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<td>rs1</td>
<td>i=1</td>
<td>simm13</td>
<td></td>
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</tbody>
</table>
**XORcc**  
Exclusive-Or and modify icc  
**XORcc**

**Operation:**
\[ r_{[rd]} \leftarrow r_{[rs1]} \text{ XOR } (r_{[rs2]} \text{ or sign extnd(simm13)}) \]
- \( n \leftarrow r_{[rd]} <31> \)
- \( z \leftarrow \text{if } r_{[rd]} = 0 \text{ then } 1, \text{ else } 0 \)
- \( v \leftarrow 0 \)
- \( c \leftarrow 0 \)

**Assembler Syntax:**
\[ \text{xorcc } \text{reg}_{rs1}, \text{reg}_{or_imm}, \text{reg}_{rd} \]

**Description:**
This instruction does a bitwise logical XOR of the contents of register \( r_{[rs1]} \) with either the contents of \( r_{[rs2]} \) (if bit field \( i=0 \)) or the 13-bit, sign-extended immediate value contained in the instruction (if bit field \( i=1 \)). The result is stored in register \( r_{[rd]} \). XORcc also modifies all the integer condition codes in the manner described above.

**Traps:**
none

**Format:**

```
  31 30 29 25 24 19 18 14 13 12  5  4  0
  1  0  rd  0 1 0 0 1 1  rs1  i=0 ignored  rs2

  31 30 29 25 24 19 18 14 13 12  0
  1  0  rd  0 1 0 0 1 1  rs1  i=1 simm13
```